Experimental Investigation of Microwave Vulnerabilities in CMOS Inverters

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Collaboration

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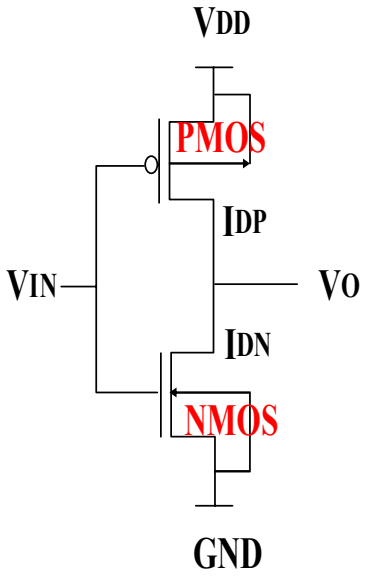
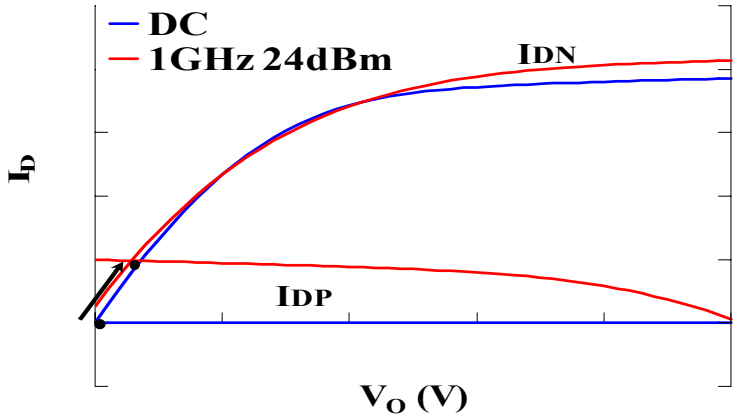
Introduction

- In this part of the work we focus on pulsed microwave interference effects on single CMOS inverters, the fundamental building block of logic ICs, consisting of an NMOS and a PMOS transistor. The inverters were designed in our group and fabricated in the AMI-1.5μm MOSIS line, both as discrete elements and as clusters of two, three, and four. Typical device geometries were: NMOS (W/L=3.2/1.6um) and PMOS (W/L=9.6/1.6), packaged and unpackaged. Here we focus on single elements.
- Our previous presentation on individual NMOSFETs showed that injected pulsed microwave power significantly affected output voltage levels between 1 and 4 GHz. Effects resulted in significant increase in drain current, development of DC offset currents at zero drain bias, reduction in breakdown voltages, substantial changes in the operational small and large signal parameters, bit flipping, and loss of saturation.The power effects were observed to be suppressed at higher frequencies.
- In this part of the work we have isolated serious vulnerabilities, that result from:
- The onset of the Parasitic Bipolar Action effect (latch-up)
- The degradation of inverter parameters and characteristics, including gain, switching capability, operational point, current/voltage offsets, power dissipation, noise margins, shifts at inflection point, peak output current instability, and
- An important new “bit-flip” error for pulses occurring at Vt state of inverter.

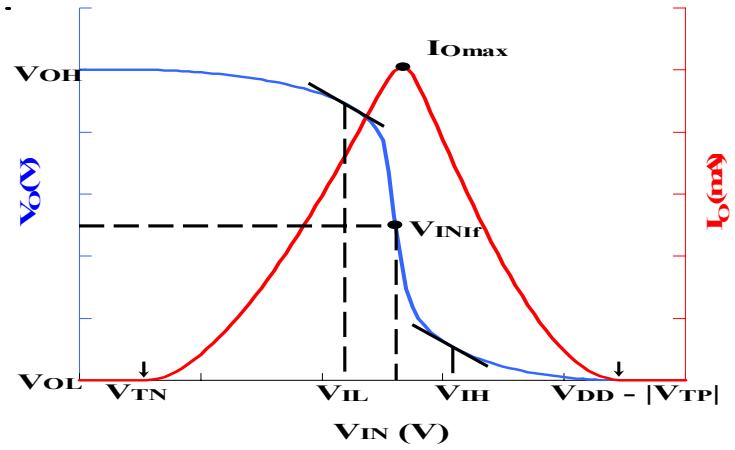
CMOS Inverter Gates

- *Parameters affected*:
- *Electronic:* Affects points of intersection of the I-V lines, transfer characteristic of gate, response time, noise margins, power dissipation, gain, large and small signal performance, and power supply rails.
- *Physical:* Gate oxides, junction boundaries, metallizations.



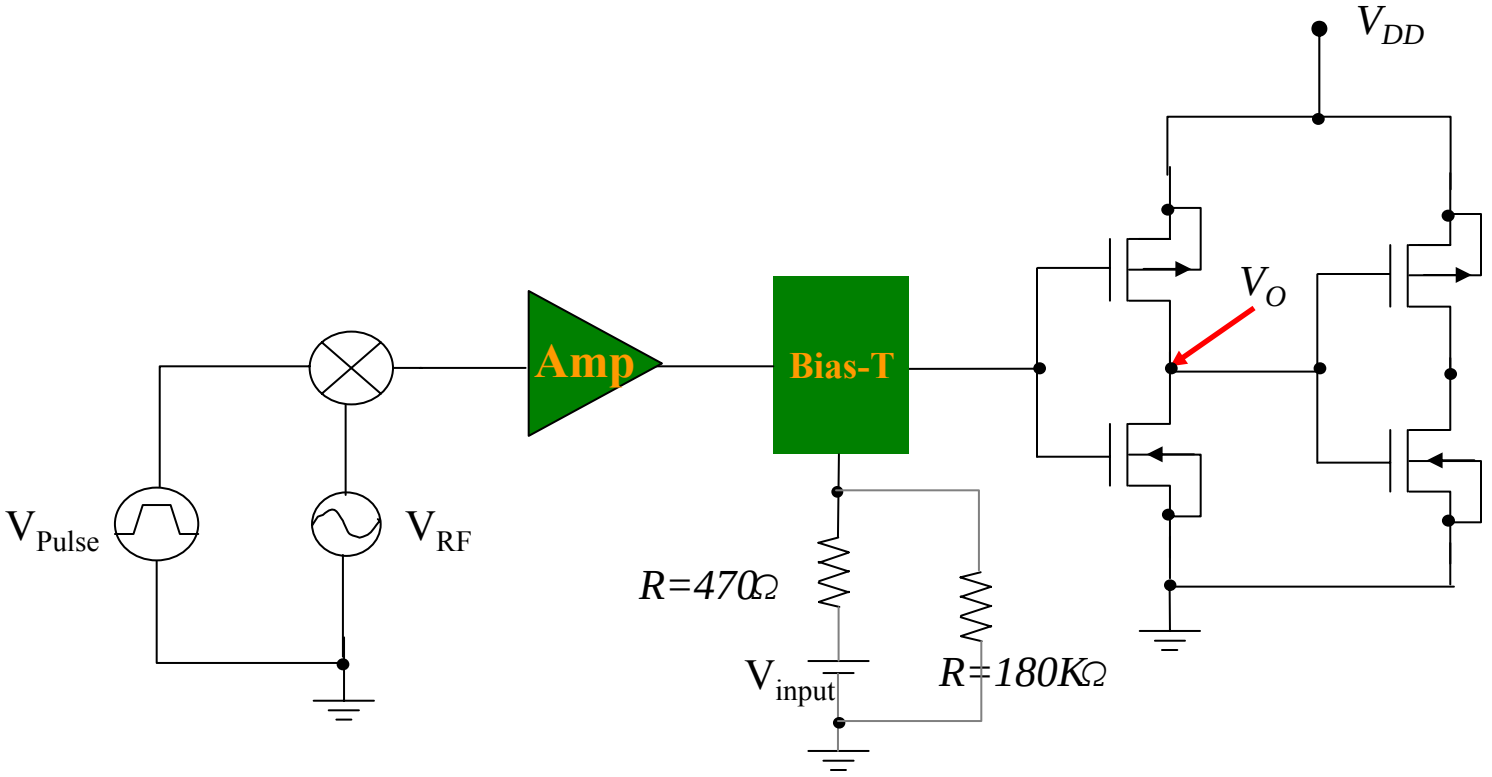


Inverter Load Characteristics



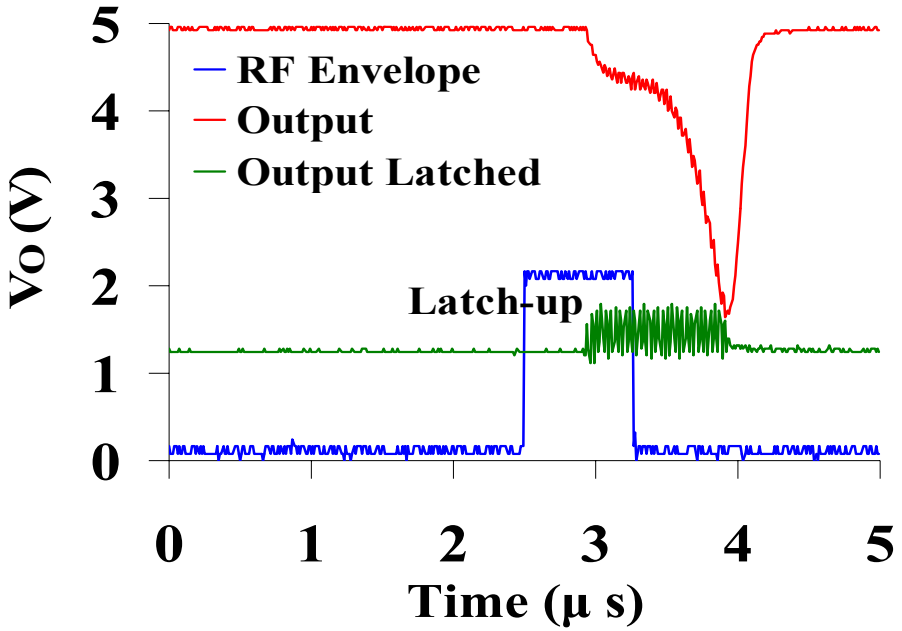
Inverter Voltage & Current Transfer Characteristics

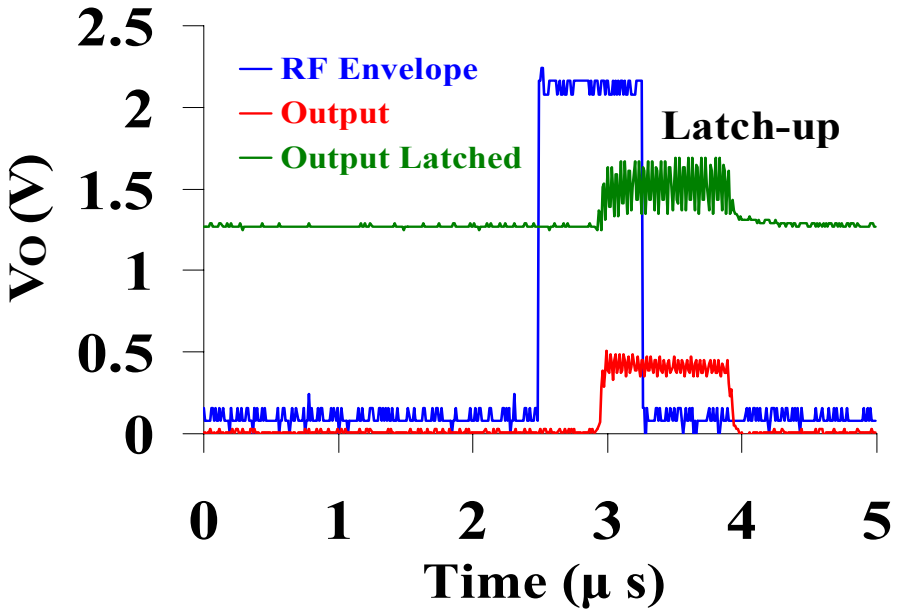
Inverter Test Set-up for Time Domain Output



- Inverter with PMOS W/L = 9.6μm/1.6μm NMOS W/L=3.2μm/1.6μm.
- RF pulse parameters: period 800ns, width: 10ms, frequency: 1.23 ~ 4GHz, power: 0dBm ~ 28.9dBm.

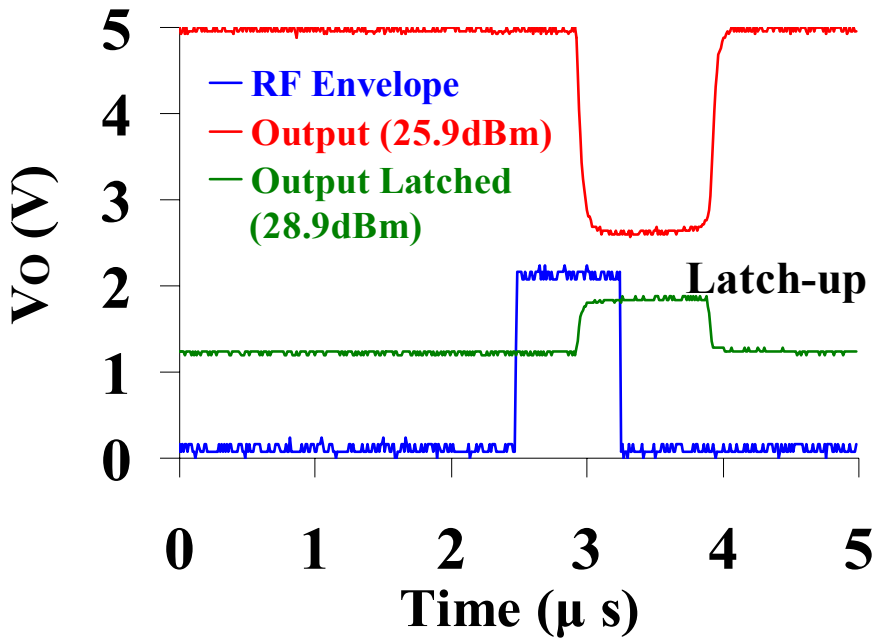
Pulsed RF Injection at Inverter Input: 1.23 GHz

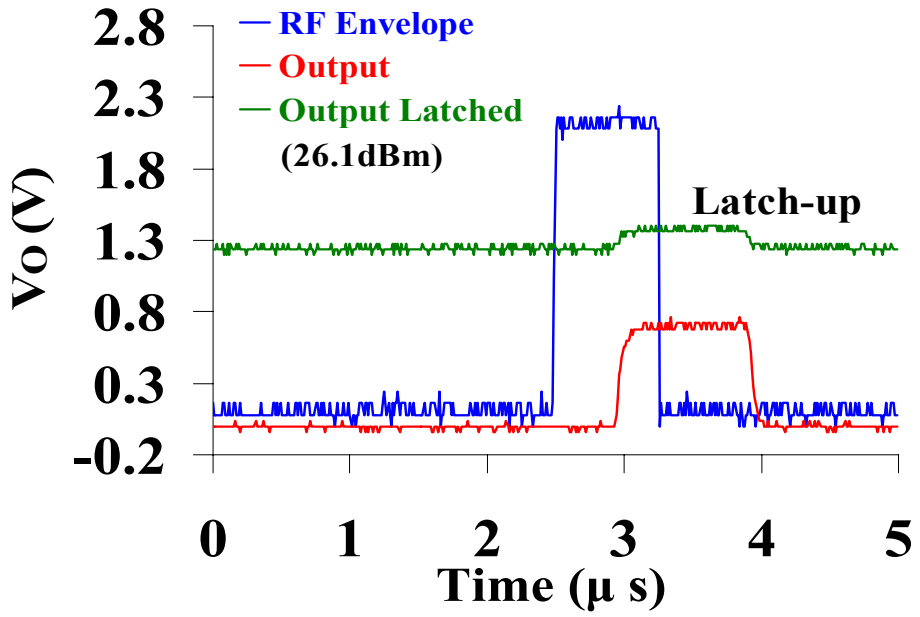




- Pulse width 800ns, period 10ms.
- At 20 dBm and 1.23 GHz no Latch-up is observed.
- At 22.45dBm and frequency 1.23GHz, with input state low (0V), output of inverter (1) shows gradual decrease with repeated pulses until complete latch-up is observed (1.24V).
- Input logic state high (5V DC). The output DC level increases as RF power increases. At 23.25dBm, the CMOS inverter experiences latch-up of output to 1.24V. Device bias (V_{DD}) needs to be reset to get normal operation again.

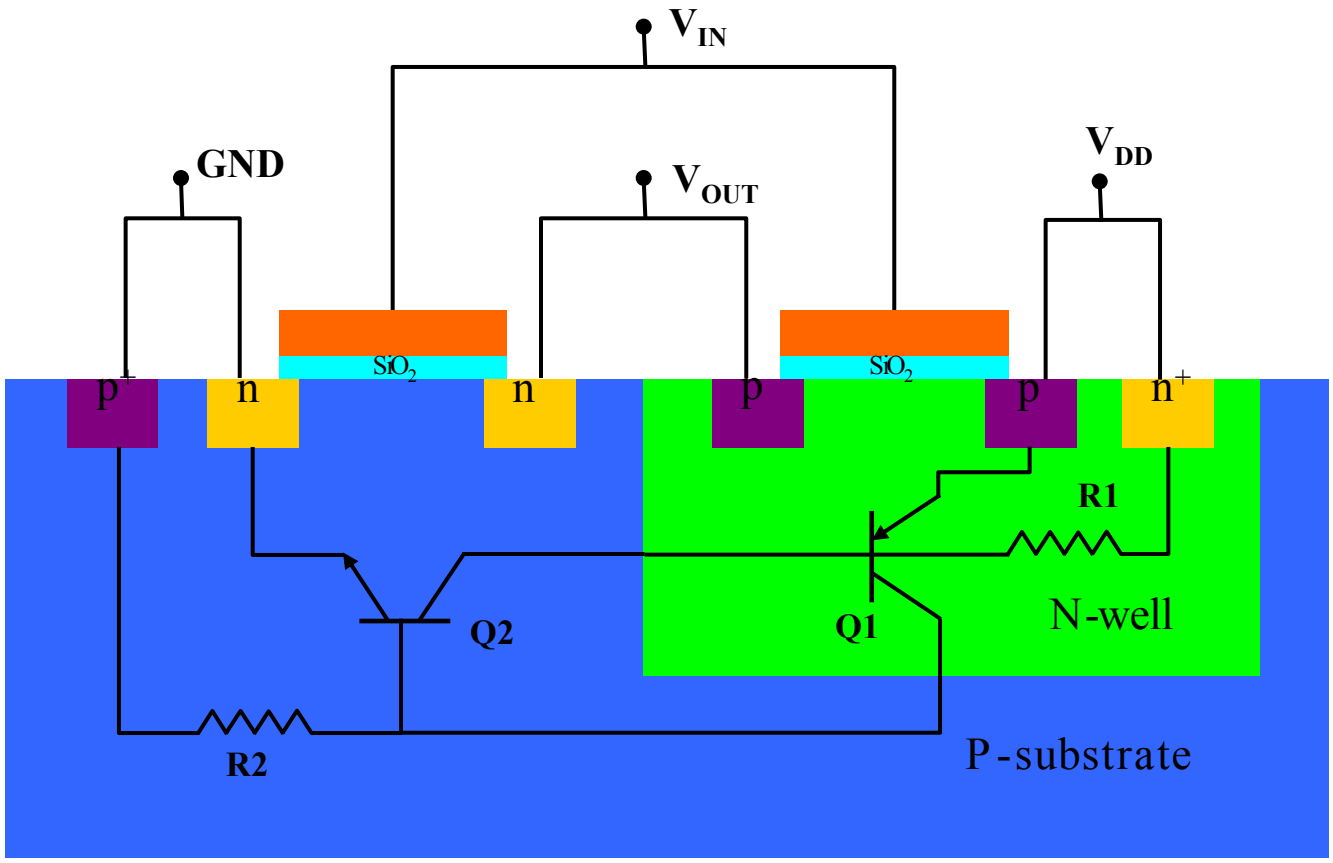
Pulsed RF Injection at Inverter Input: 4 GHz





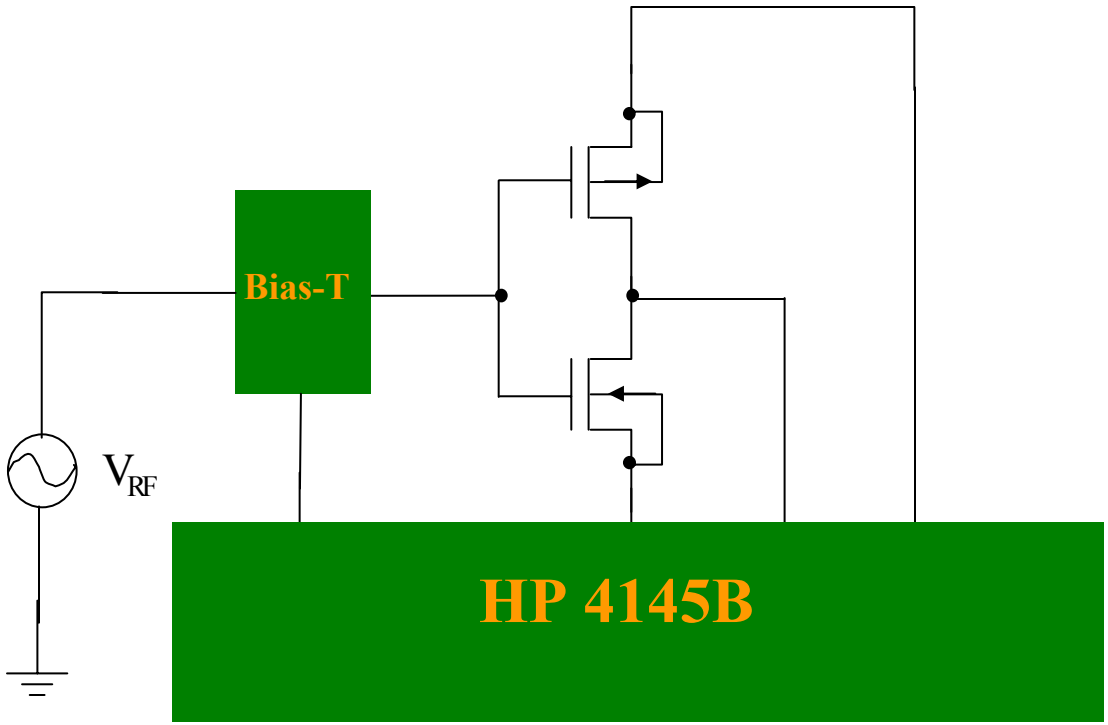
- Input logic state low (0V DC): Output (25.9dBm) flips to ~1/2V_{OH}. At 4GHz increased RF power 28.9dBm is needed to cause latch-up.
- Input logic state high (5V DC): at 4GHz, the CMOS inverter experiences latch-up at higher power (26.1dBm).

Parasitic Bipolar Transistor Action in CMOS inverters



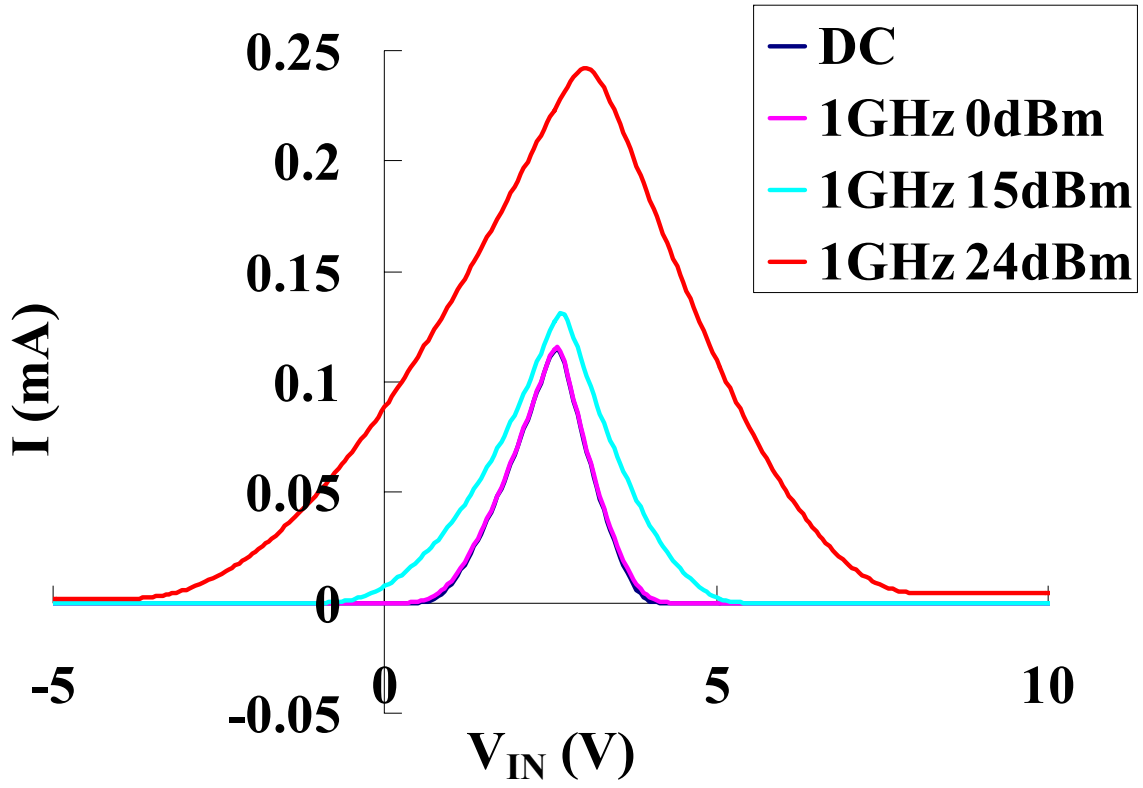
- If external applied voltages exceed V_{LU} or if enough charge exists in the n or p wells, then Q1, Q2 bipolars turn on causing significant currents (mA) to flow in the parasitic bipolar transistor loop, thus incapacitating the channel path.
- Depending on inverter fabrication parameters (junction and well doping, Si resistivity) the parasitic β can become very important.
- This new path of conduction will virtually stop CMOS action rendering the inverter inoperable.
- These bipolar currents can become high enough to damage permanently, especially if V_{DD} is not well regulated.

Inverter Test Set-up for I-V Characteristics



- Inverter with PMOS W/L = 9.6μm/1.6μm NMOS W/L=3.2μm/1.6μm.
- RF condition : Frequency : 800MHz -3GHz. Power: 0 - 24dBm.

Inverter IO-VIN transfer characteristic with power at 1GHz



IO-VIN transfer characteristic shows large current increase with power level.

NMOS and PMOS devices can not be turned ON or OFF due to excess charge in channel.

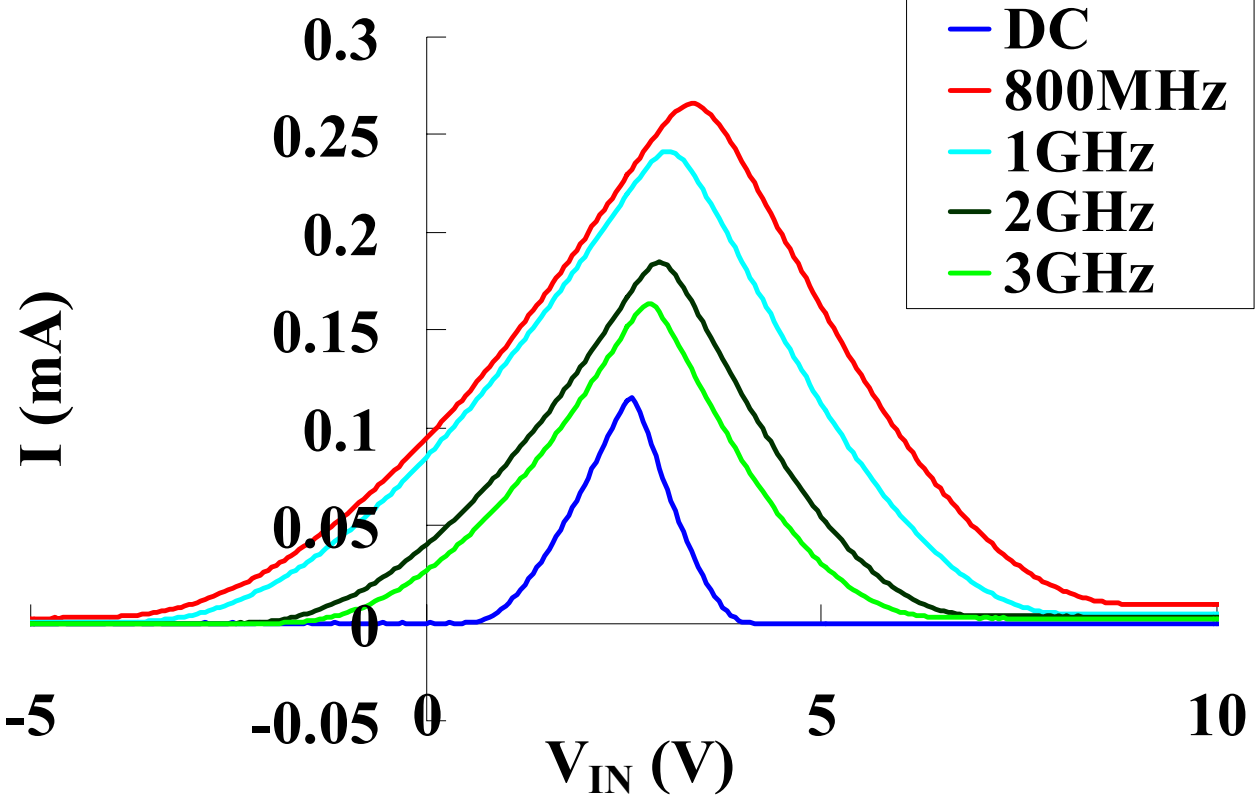
Power dissipation on "stand-by" ON or OFF state becomes excessive.

Max current point shift is observed.

Power dissipation at "stand-by":

(a) at DC: negligible power dissipation at ON and OFF state. (b) at 1GHz 15dBm power dissipation= 0.14μW (ON state) and 0.015μW (OFF), Asymmetric response (c) at 1GHz 24dBm power dissipation =20.9μW (ON) and 31.9μW (OFF) state.

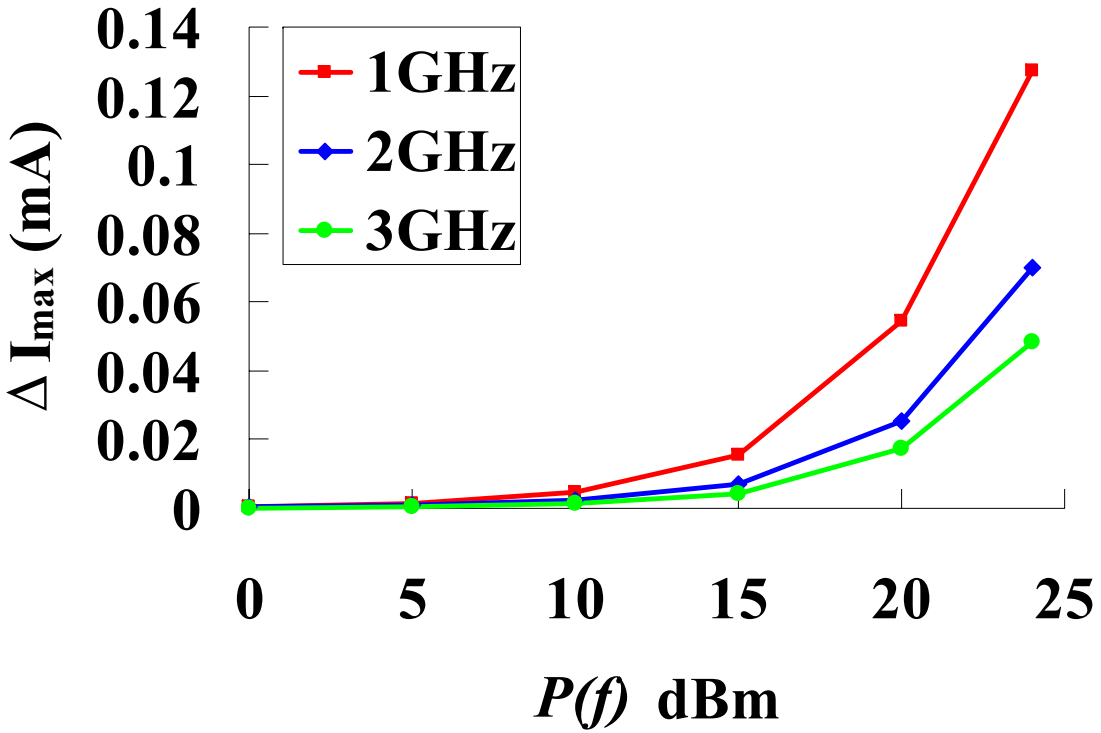
Inverter Io-VIN Transfer Characteristic with Frequency at 24dBm



Power effect is suppressed with increasing frequency. still degradation in inverter characteristics has been observed.

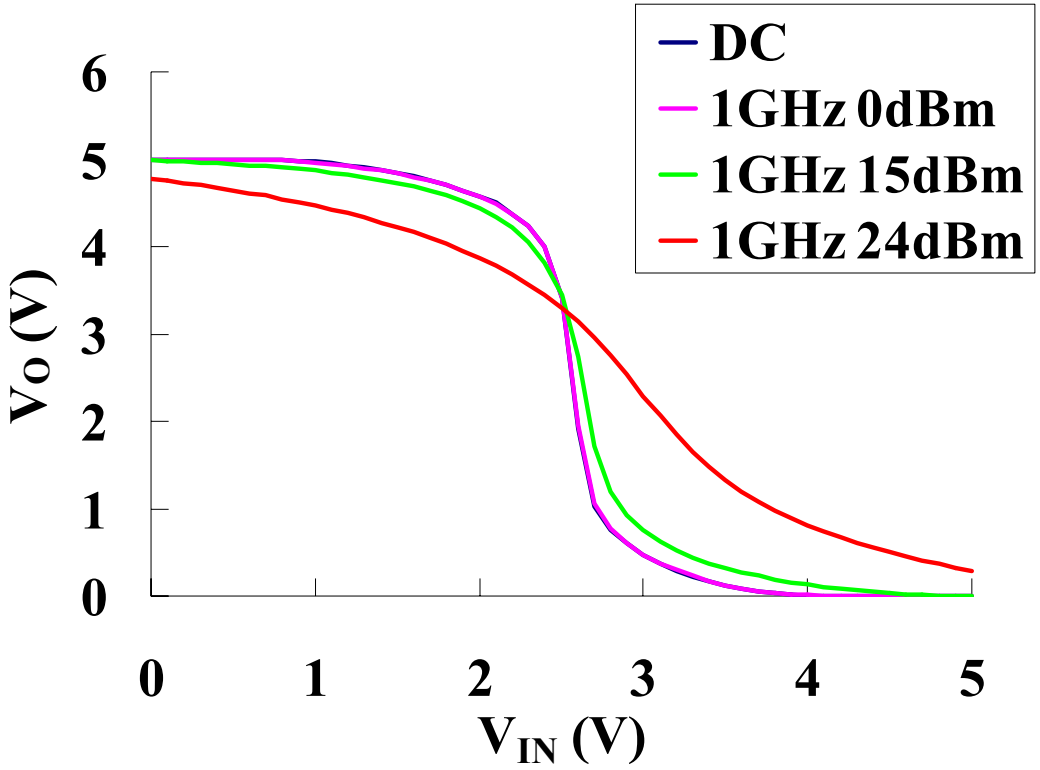
Shift of I_{omax} observed

I_{Omax} Change with RF Power and Frequency



- $\Delta I_{Omax} = I_{Omax}(RF) - I_{Omax}(DC)$
- Huge increases in I_{Omax} are observed with power level.
- Inverter suffers large dynamic power dissipation (on switching), in addition to "stand-by" dissipation.

Inverter Transfer Characteristics with Power at 1GHz



Noise Margin degradation :

DC: NMH=VOH – VIH = (5 – 2.9)V=2.1V,
NML= VIL – VOL = (2.3-0)V =2.3V.

1GHz 15dBm: NMH=(5-3.4)V=1.6V,
NML=VIL-VOL=(2.1-0)=2.1V.

1GHz 24dBm: NMH=0.97V, NML=1.81V.

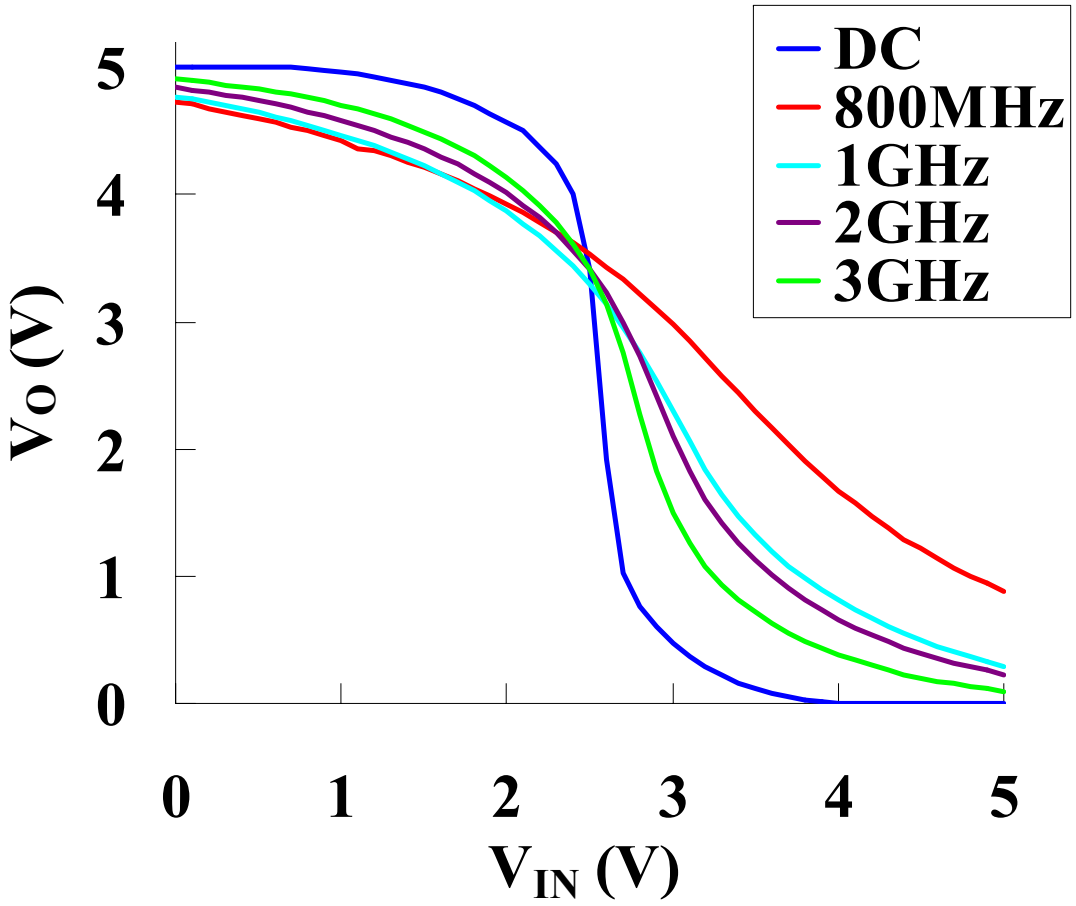
Gain degradation:

DC: 11.985 V/V

1GHz 15dBm: 5.776V/V

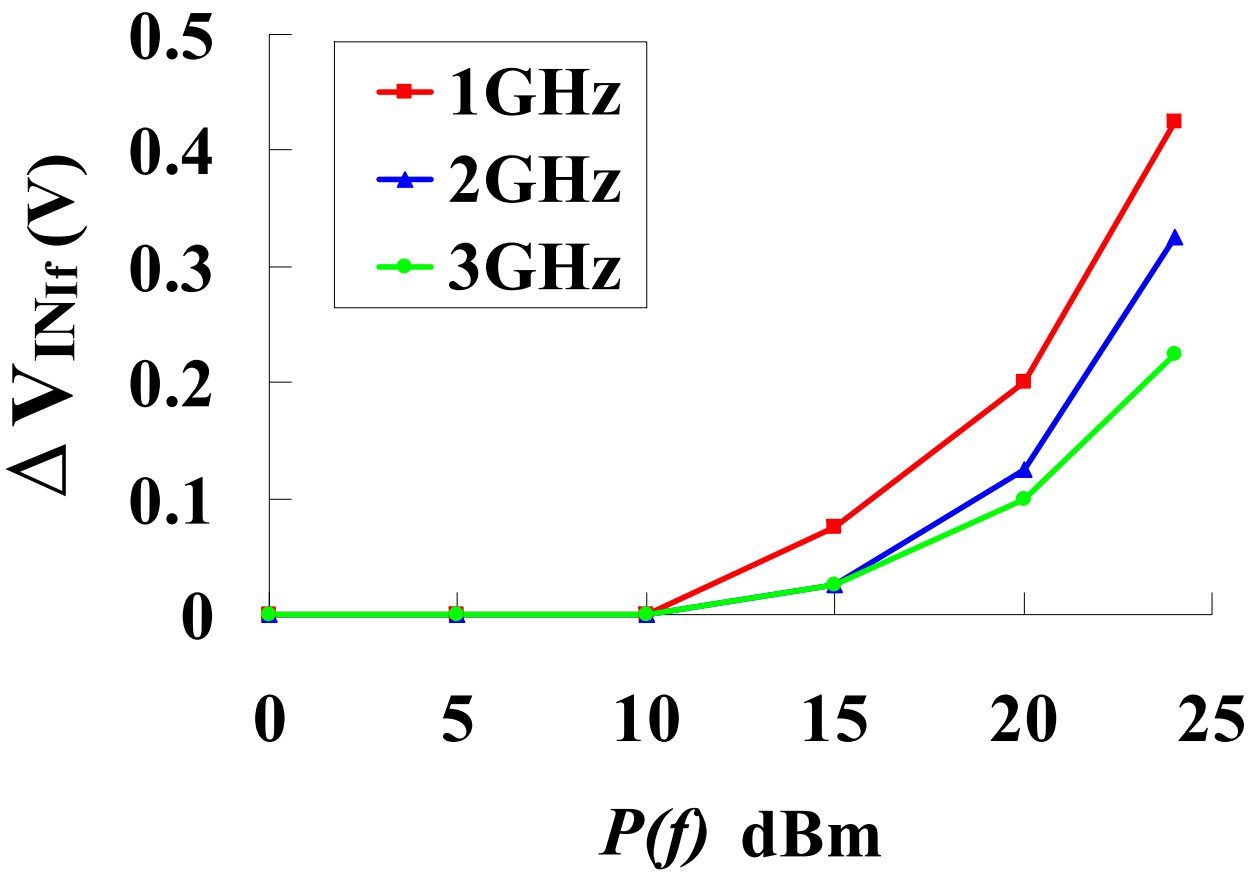
1GHz 24dBm: 2.08V/V

Inverter Transfer Characteristics with RF frequency at 24dBm



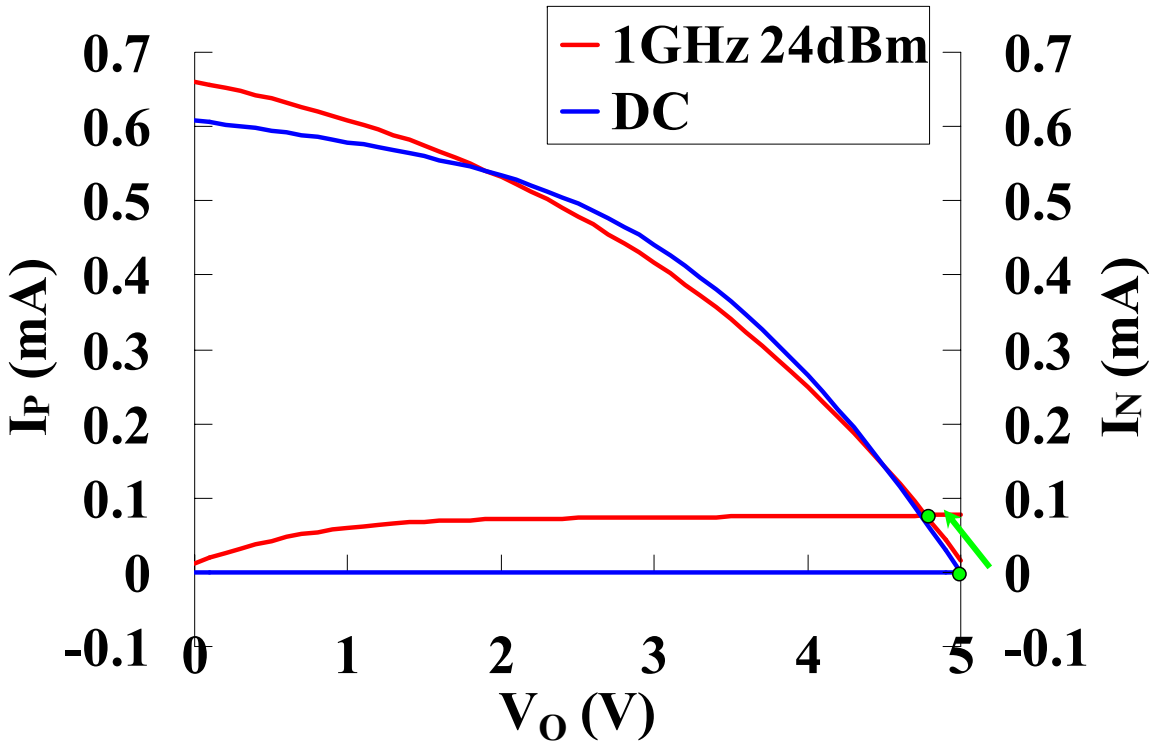
Power effect suppressed with increasing frequency

Inflection Point Shift with RF Power and Frequency



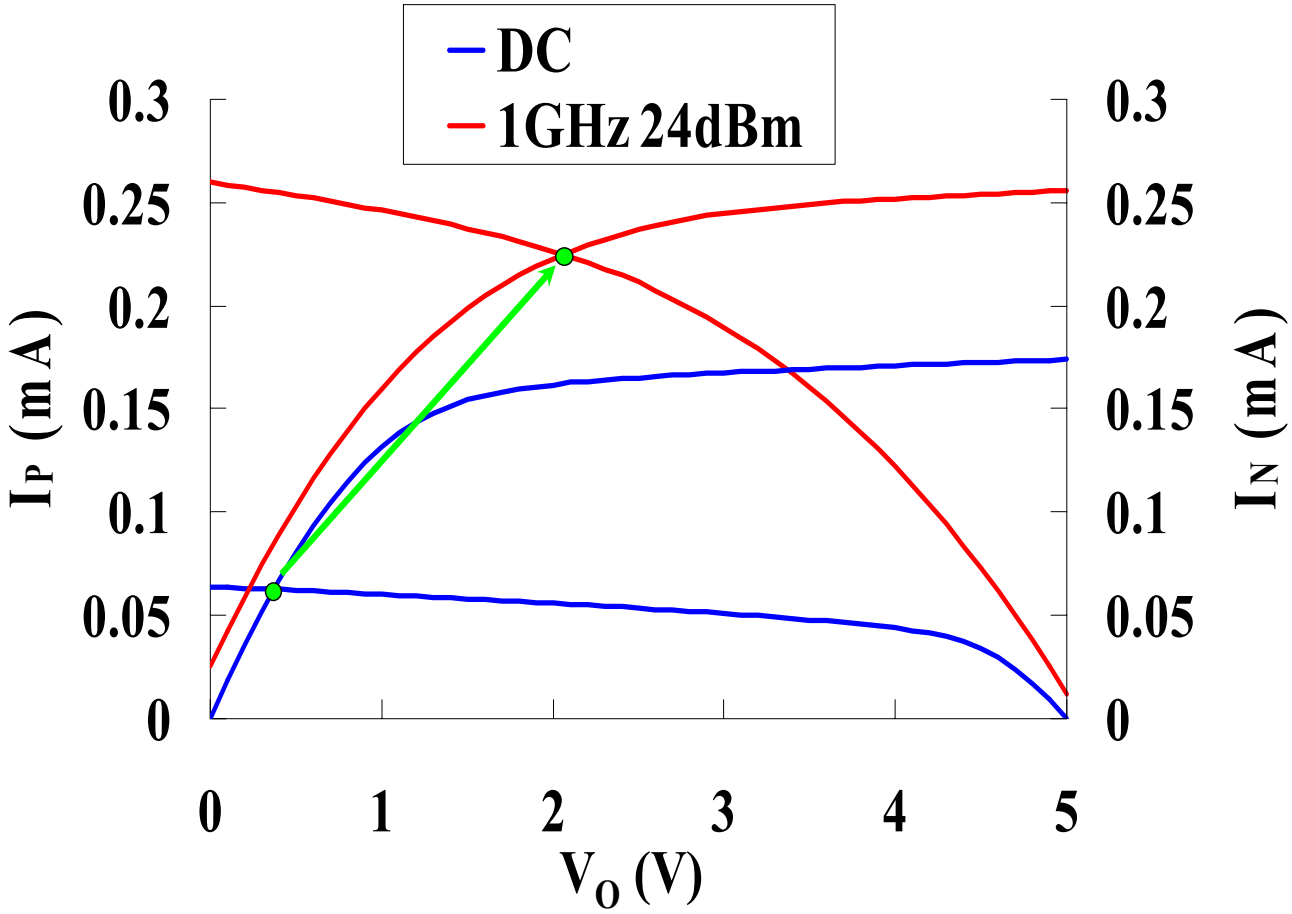
- Inflection point shift increases with power level.
- $\Delta V_{INIf} = V_{INIf}(RF) - V_{INIf}(DC)$.
- Slope of transfer curve changes degrading gain severely

Inverter Load-line I-V Characteristics Input Low (V_{IN}=0V): 1GHz 24dBm



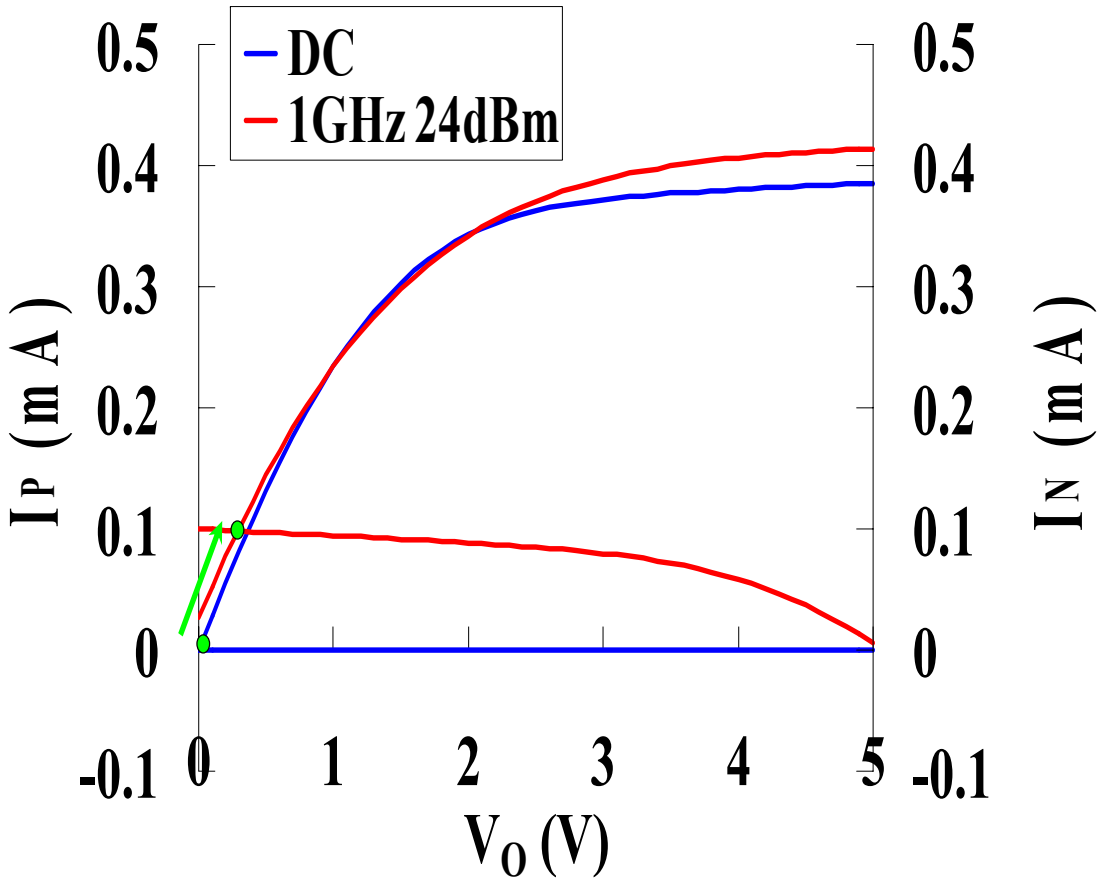
- Change in bias point results in both N and P MOS transistors "ON" changing the effective "on" resistance and capacitance and affecting switching speed and increasing propagation delays.

Inverter Load-line I-V Characteristic Input Intermmediate (V_{IN}=3.1V): 1GHz 24dBm



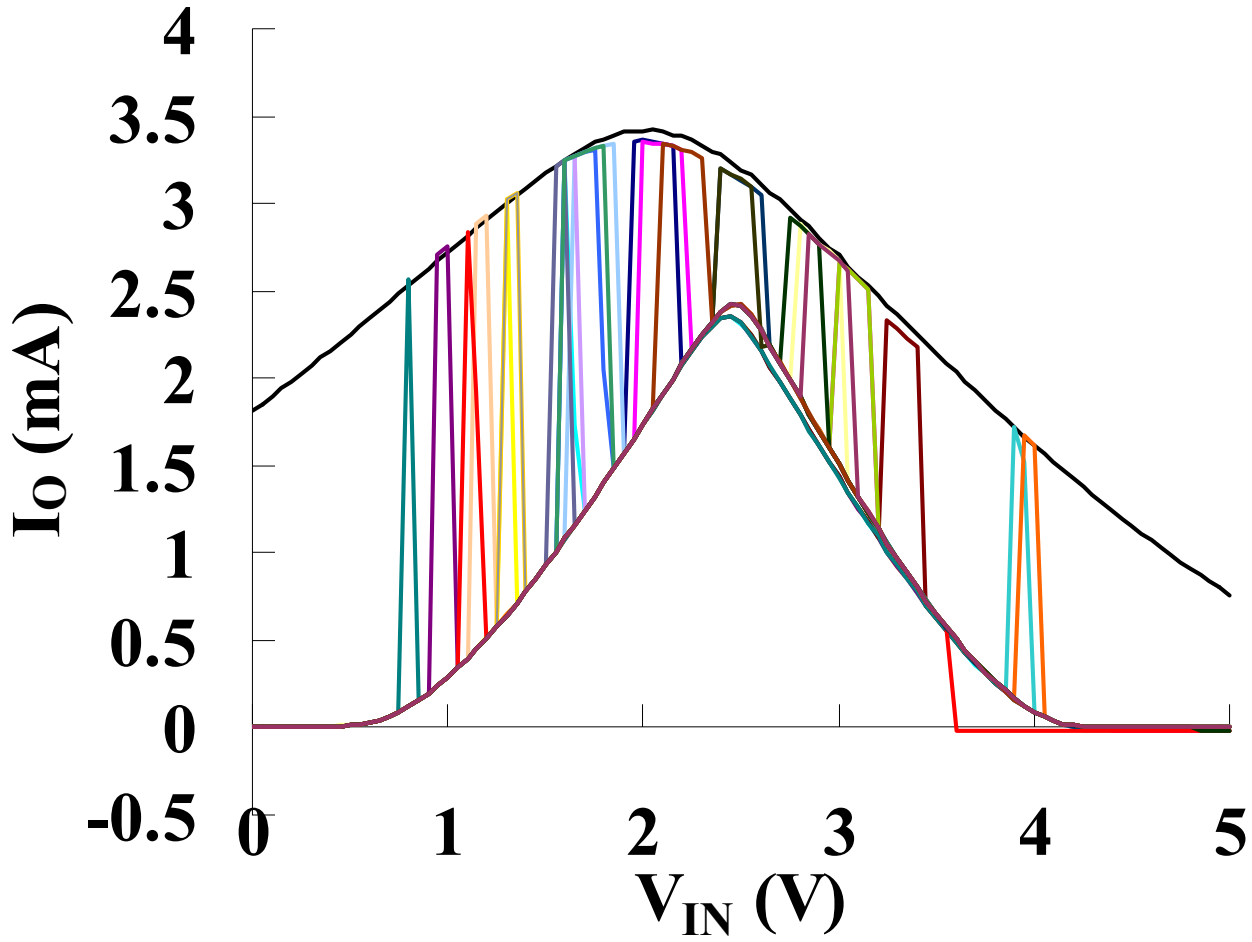
Effects are more pronounced

Inverter Load-line I-V Characteristics
Input High:1GHz 24dBm



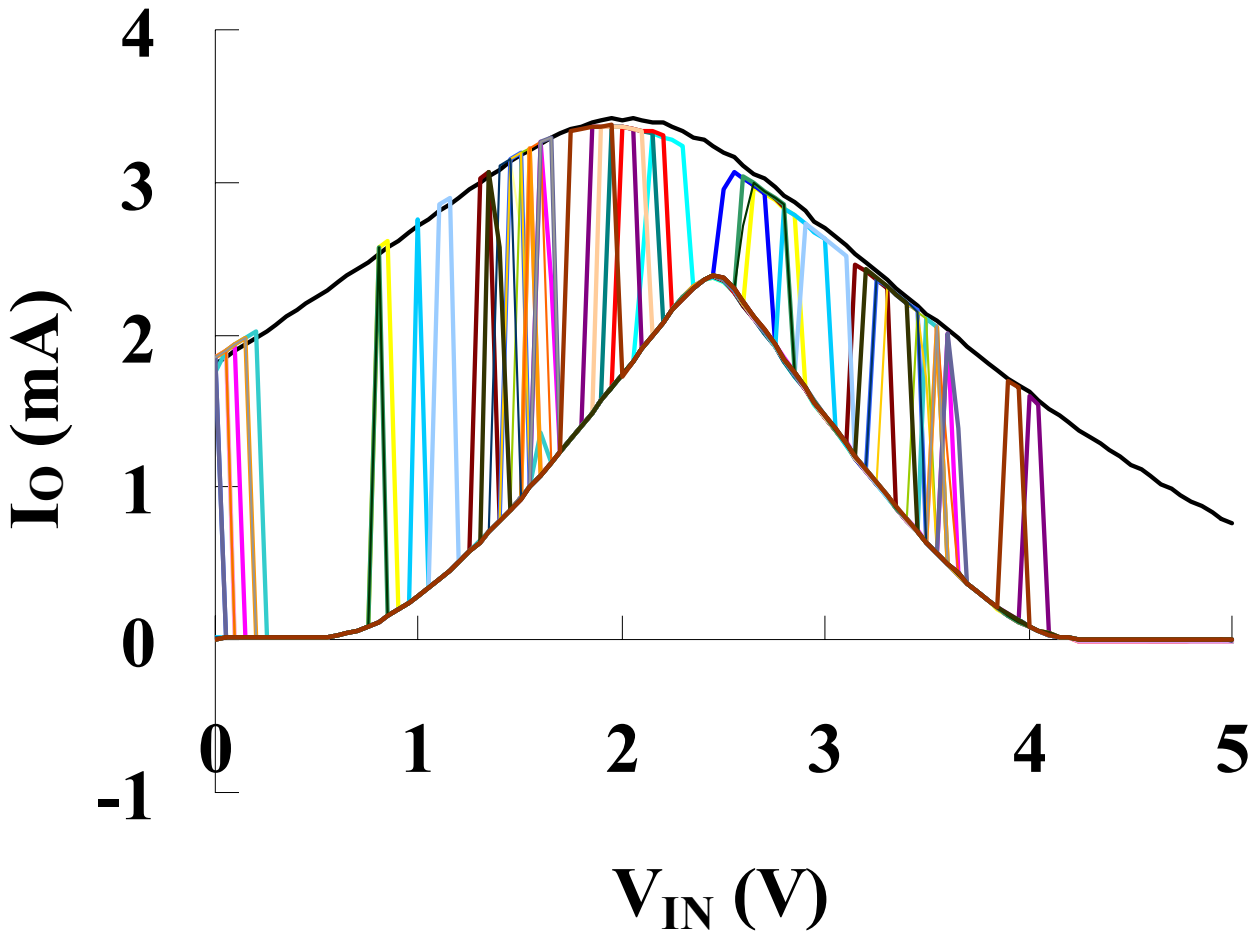
- Inverter can not be turned OFF or ON at RF power levels above 15dBm (1GHz).
- In deep sub-micron VLSI chips, where dimensions are severely scaled down, this increase in current at "stand-by" state will cause additional IR voltage drops in the interconnects from power rail to the device and the device contacts themselves, resulting in catastrophic failure with "hard errors" shutting down neighboring devices and it presents a new serious reliability problem.

1GHz 24dBm Pulsed RF (Pulse Width: 1.5ms/ Period: 2s)

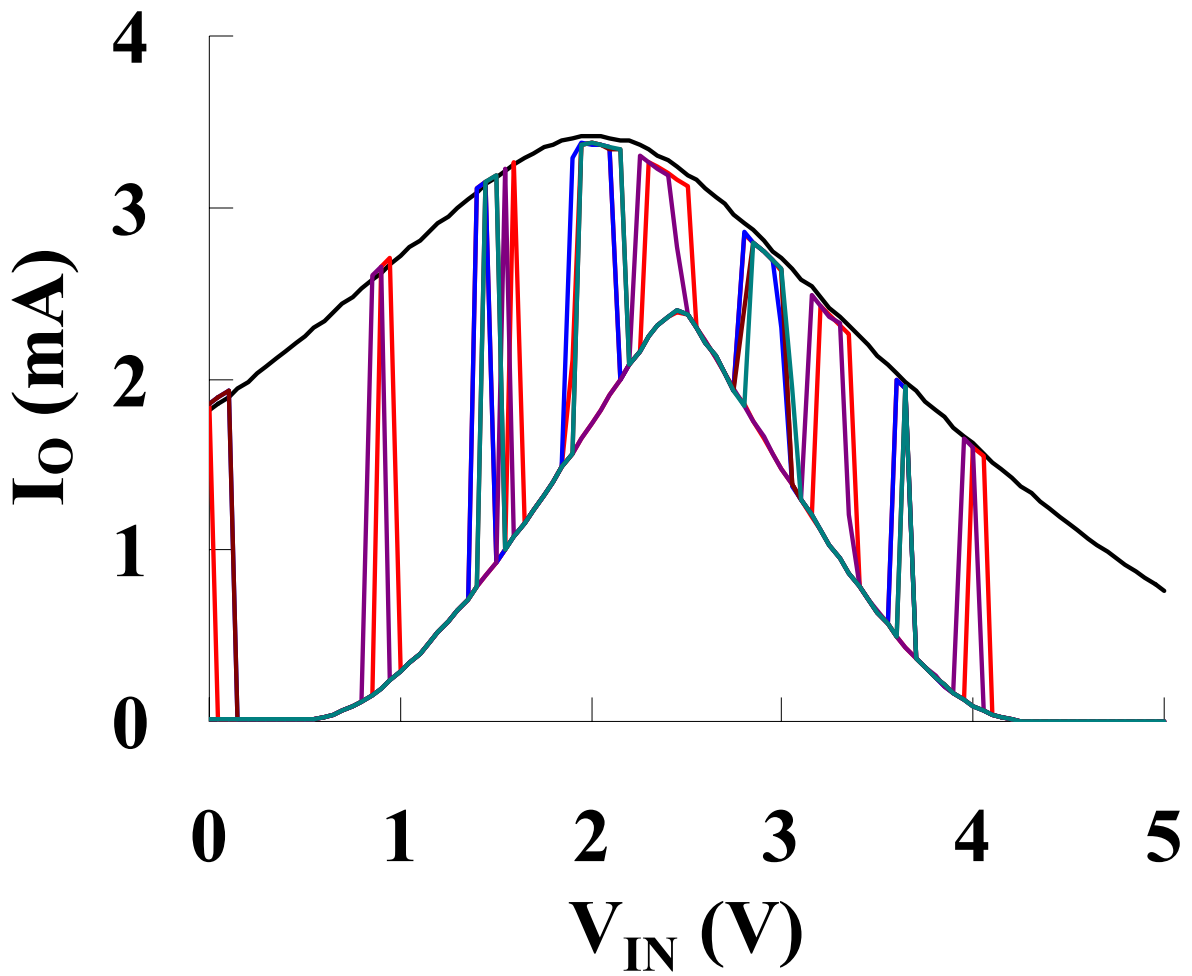


- Relative importance of thermal effects with respect to excess charges:
- Comparison of pulsed and CW measurement
- Different period/width pulses: period 200ms-2s width 1.5ms-500ms

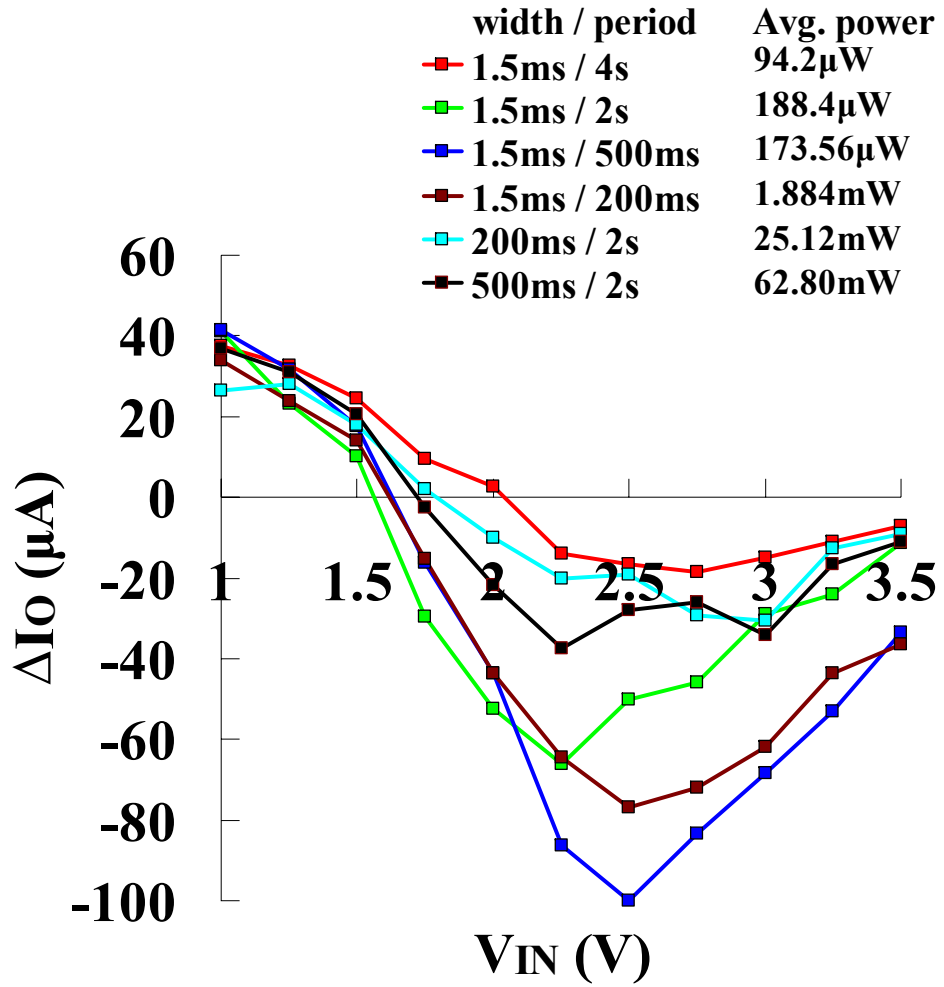
1GHz 24dBm Pulsed RF
(Pulse Width: 1.5ms/ Period: 500ms)



1GHz 24dBm Pulsed RF
(Pulse Width: 1.5ms/ Period: 200ms)

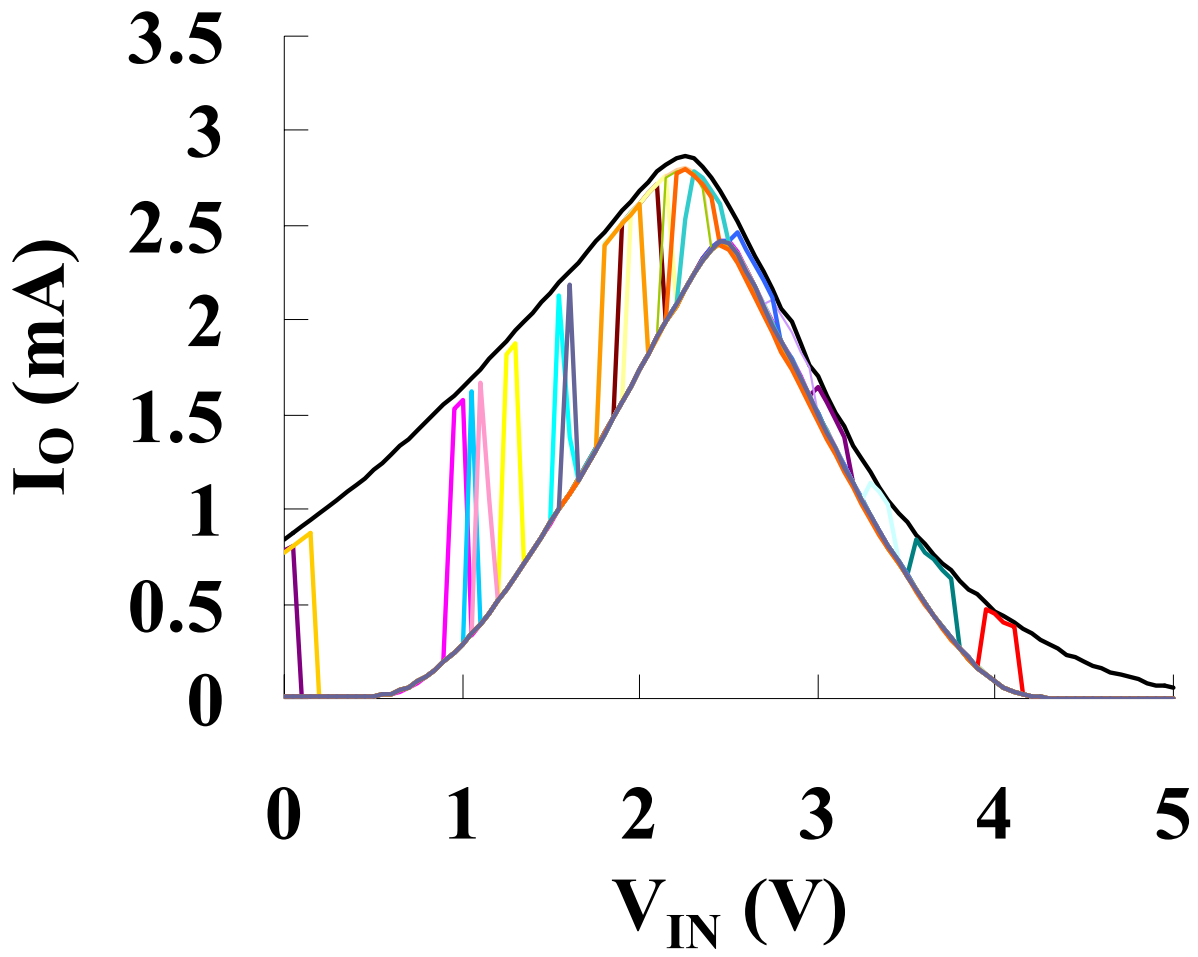


Incremental Current Change ΔIo vs VIN 1GHz 24dBm Pulses

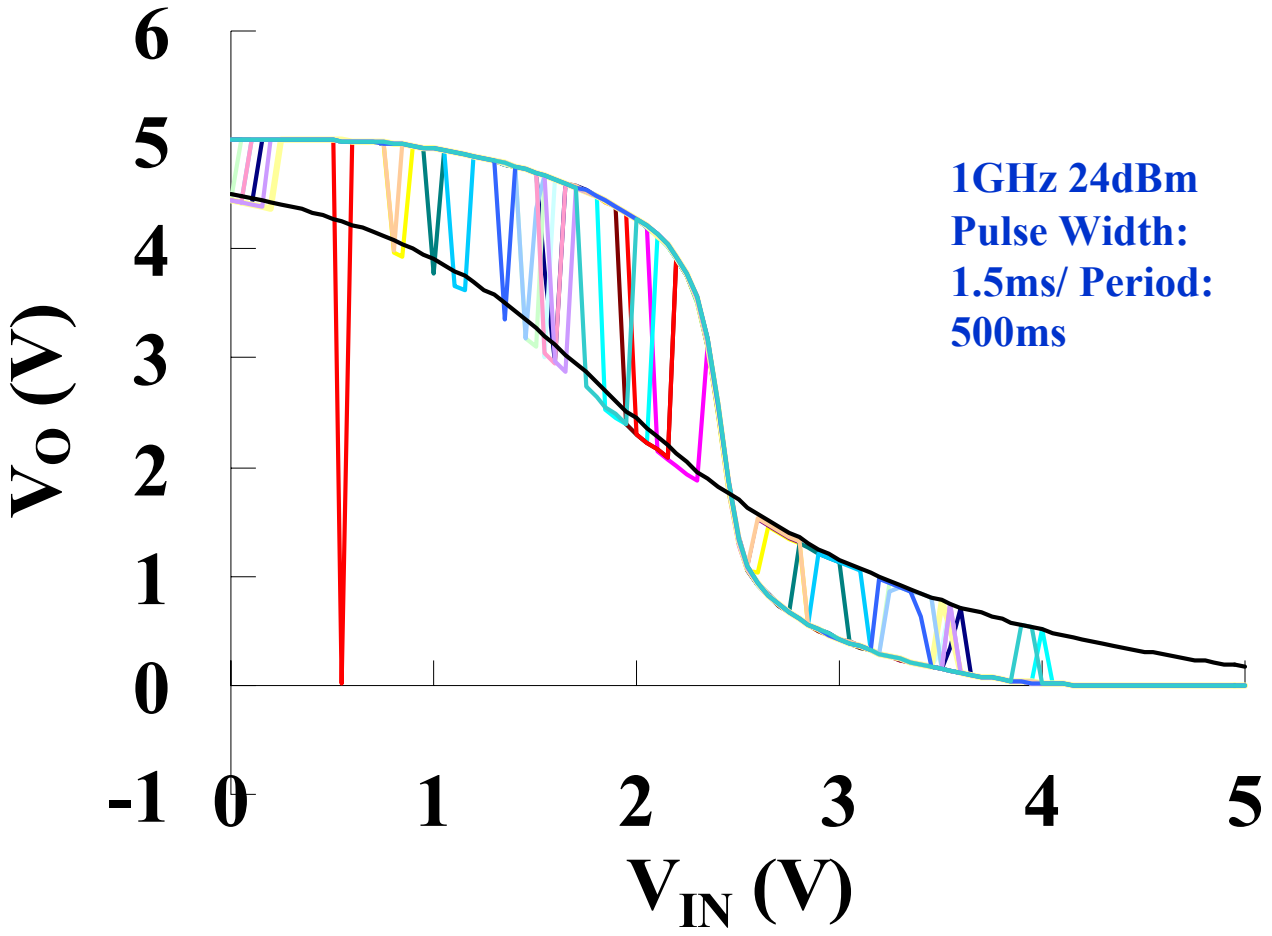


- ΔIo=Io(Pulsed)-Io(CW)
- The plot of ΔIo vs VIN from all the previous measurements shows both positive and negative values. The positive values show that current due to CW is less than that due to pulses which points to a small contribution of thermal effects due to CW.
- The negative values show that the thermal contribution is not significant for the VIN range, although at higher average pulse power some thermal effects may be in operation.
- The pulse and CW effects are predominantly due to excess charges in CMOS device.

3GHz 24dBm Pulsed RF
(Pulse Width: 1.5ms/ Period: 2s)



Voltage Transfer Characteristic at CW and Pulsed Injection

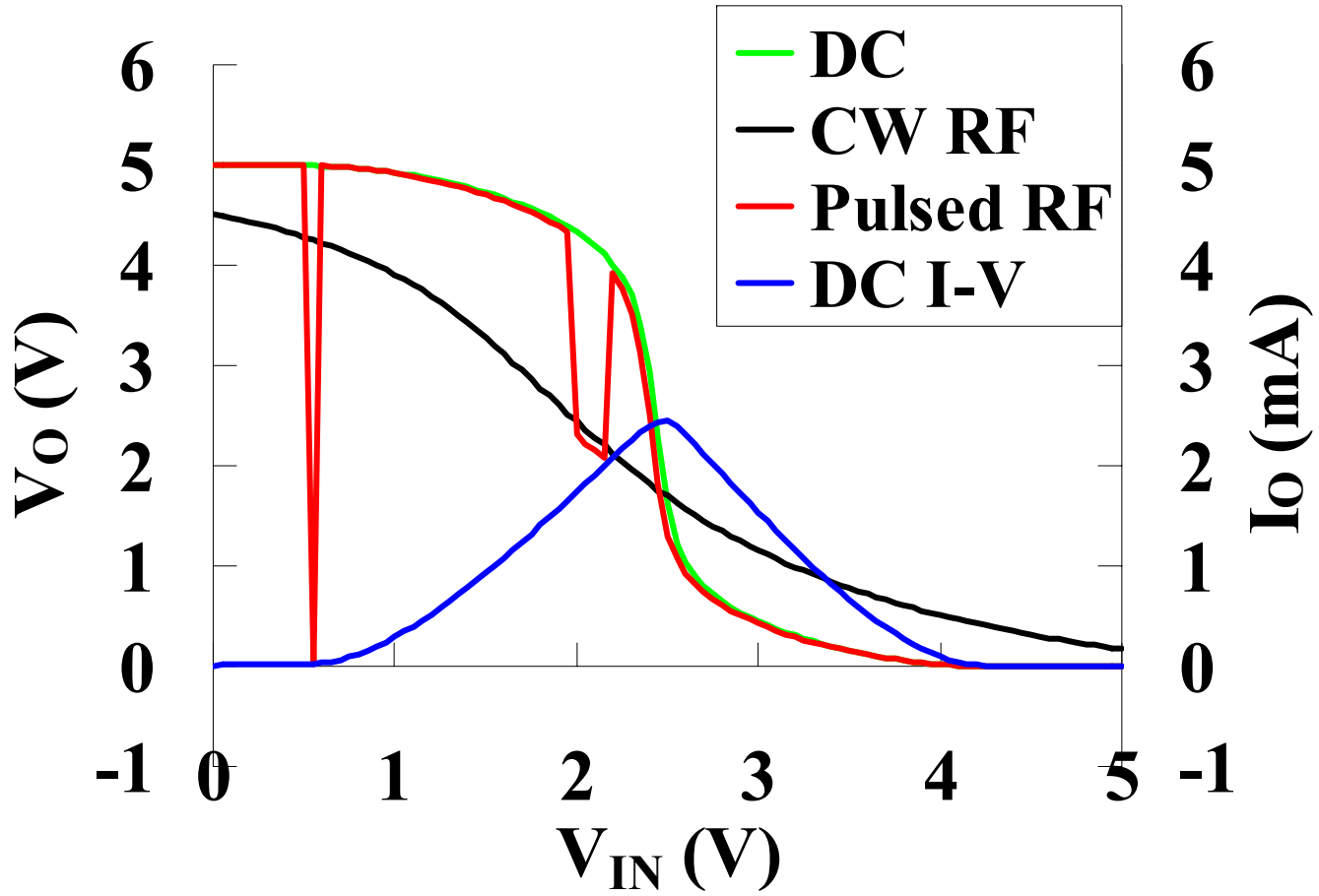


"Bit flip" error at Vt

Device are observed to flip from high to low for pulses at Vt

This is an important vulnerability as it introduces "soft" errors without permanent operational changes.

1GHz 24dBm Pulsed RF
(Pulse Width: 1.5ms/ Period: 500ms)



Summary

- CMOS inverters under pulsed RF measurements, experience severe latch-up due to excess charges turning on the parasitic bipolar action in the p-substrate-n-well CMOS structure, for power levels at or above 22.45dBm.
- Inverter characteristics showed significant degradation in the voltage and current transfer characteristics, the inverter operational point, the inverter gain, the input output voltages (VOH, VOL, VIL, VIH), the noise margins and substantial power dissipation increases due to output current increase at “on” and “off” states and dynamic power dissipation increases at the intermediate state.
- Comparison between pulsed and CW measurements showed little contribution from thermal effects.
- A new “bit flip” error under pulsed measurements was observed to happen when V_{IN} approaches the threshold voltage of the devices, and a pulse occurs. The output then flips from Hi to Lo.
- The observed substantial increase in output current at “stand-by” results in additional IR voltage drops in deep sub-micron VLSI chips, giving catastrophic failures with “hard errors” and shutting down neighboring devices. This is expected to present a new serious reliability problem and will be investigated further on deep submicron devices.
- Continuing and future work will evaluate the effects with different size (W/L) inverters, examine the effects of asymmetrical response of the devices, examine multiple inverter clusters to evaluate propagation of events, evaluate small signal parameters and switching characteristics for propagation delays and switching speed, in order to improve the inverter design to harden against pulses. Experimental results will be incorporated in model (N. Goldsman). Next step includes differential amplifier studies and guard protection using nanocomposites.