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# Nonlinear Effects in Advanced Communications Circuits Excited by Pulsed RF

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# Program Goals

- Investigate basic electronic mechanisms that cause RF-induced upset in communications circuits
- Characterize device-level effects
- Identify how susceptibility depends on:
  - RF power, frequency and modulation
  - Device type, voltage, size, layout, parasitic elements, etc.
  - Scaling laws: future devices will be smaller, faster, lower voltage
- Develop basis for modeling RF effects

# Outline

- Overview of basic circuit elements excited by RF
- Characterization of nonlinear and high frequency response
- How upset depends on:
  - Input DC bias (Vbias) and supply (Vcc) voltages
  - RF characteristics (frequency, amplitude and modulation)
  - Logic family, ESD type and topology,
  - Chaotic excitation
- High frequency circuit modeling using PSPICE
- Nonlinear effects in wireless communications
- Summary of accomplishments and future directions

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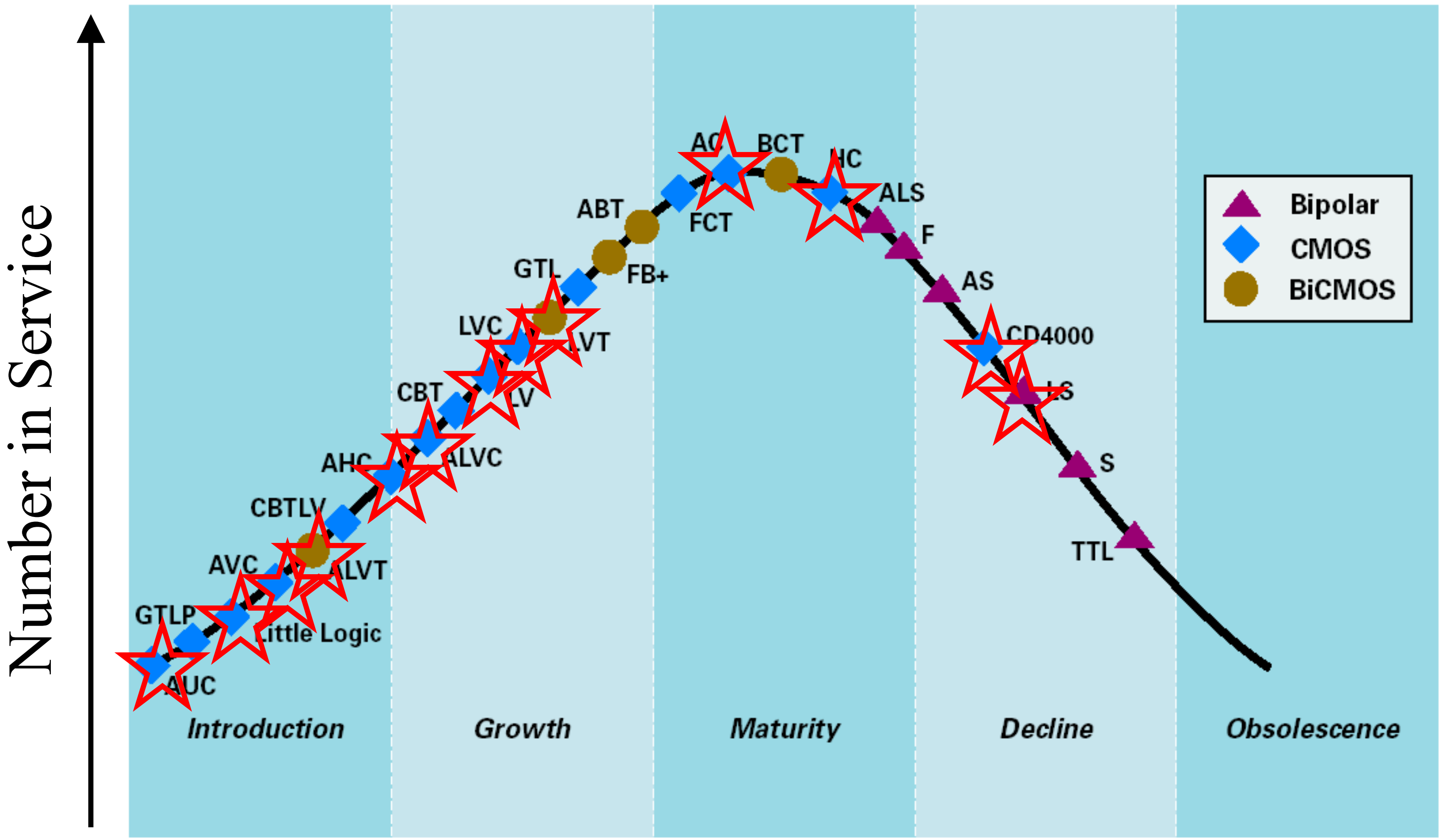
# Logic Families Tested at UMD




Source: “Logic Reference Guide,” Texas Instruments Inc., 2002.

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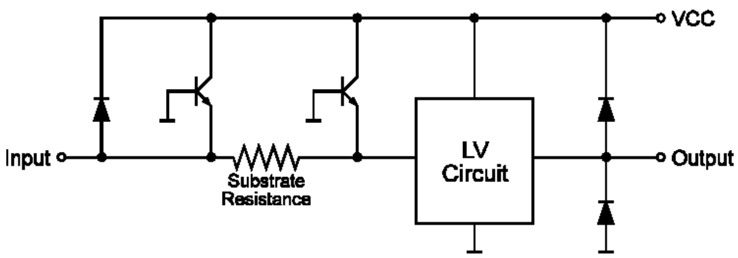
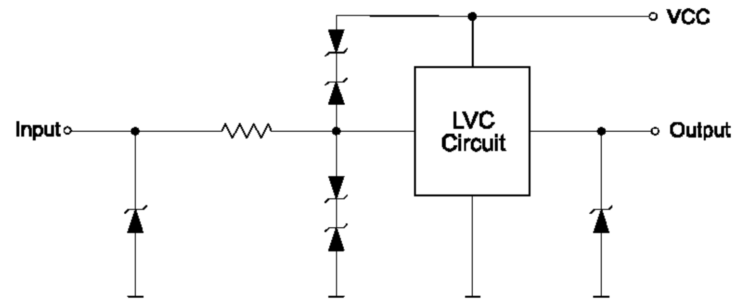
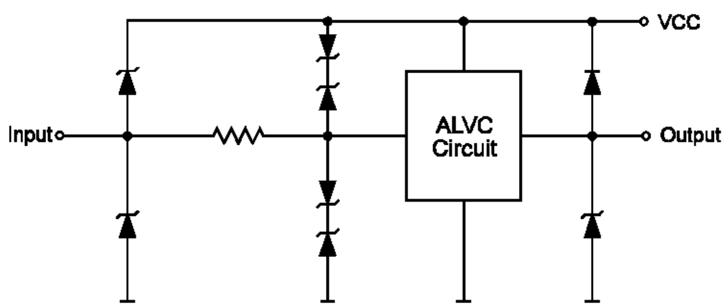
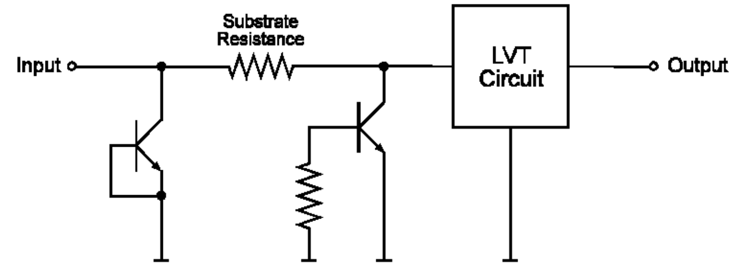
# Examples of Electrostatic Discharge (ESD) Protection Circuits in Advanced Logic



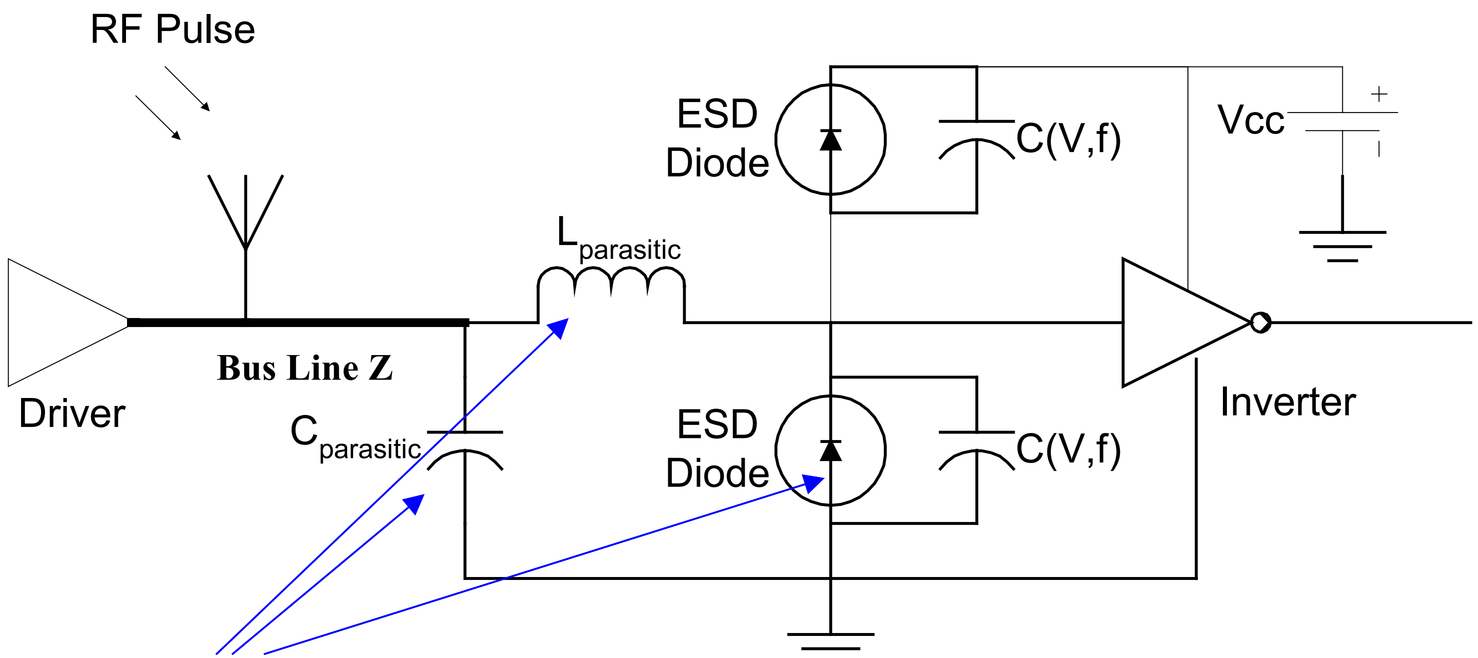



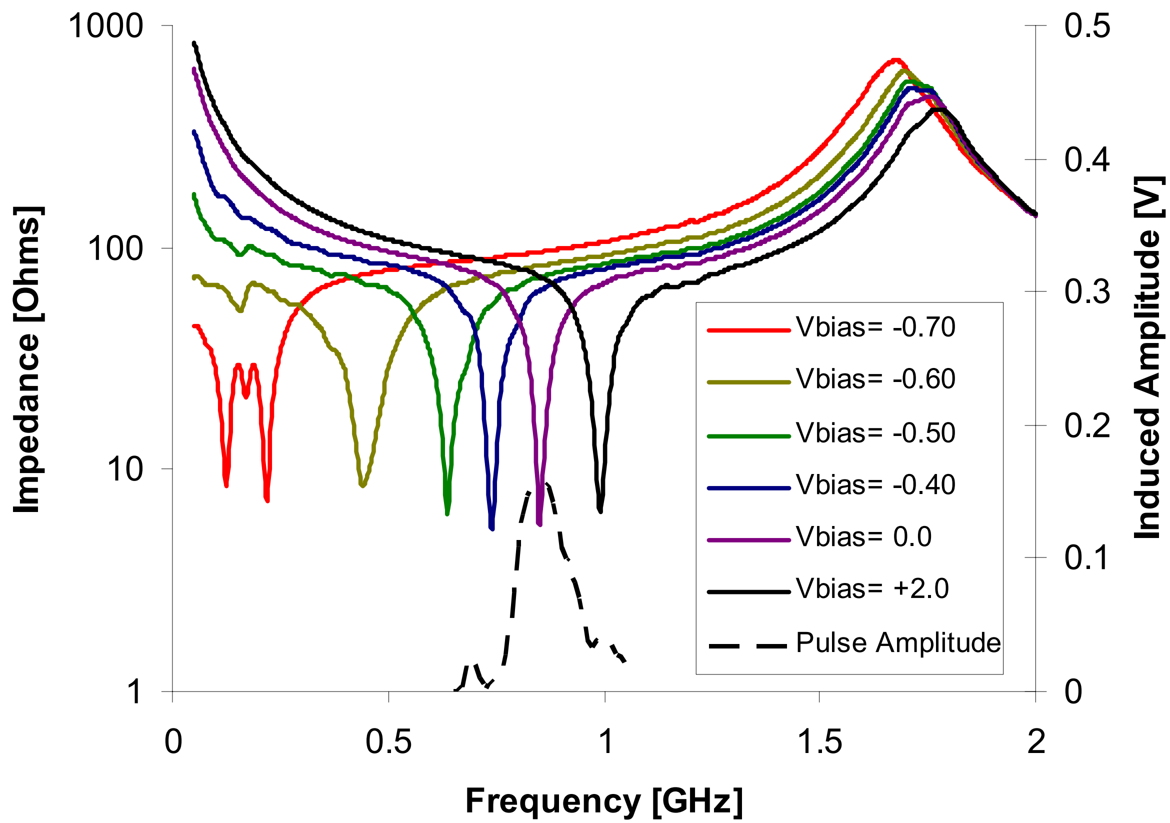

Virtually all integrated circuits have some sort of ESD.

# Consider What High Frequencies See

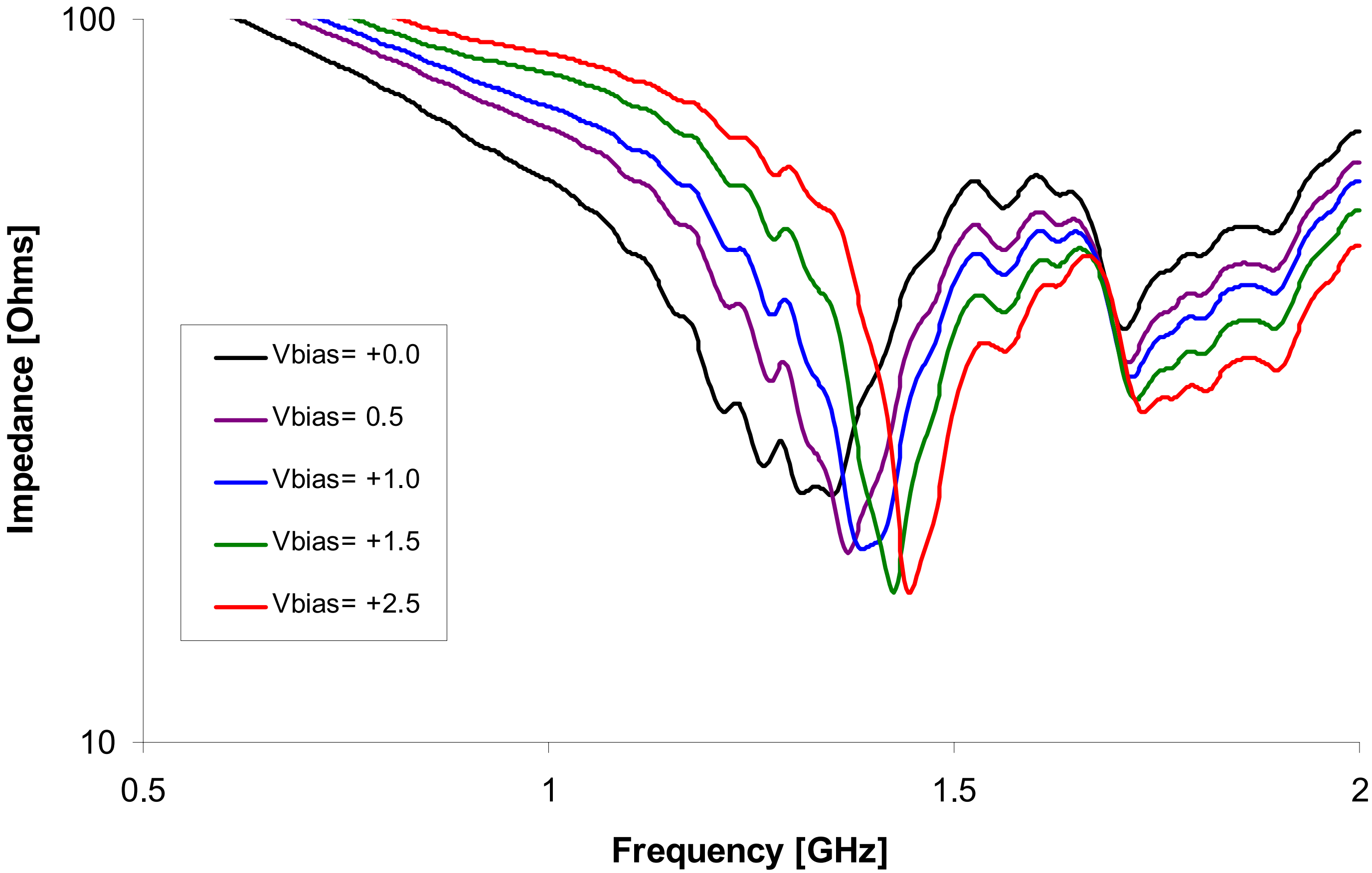



Typical circuit values are resonant at microwave frequencies

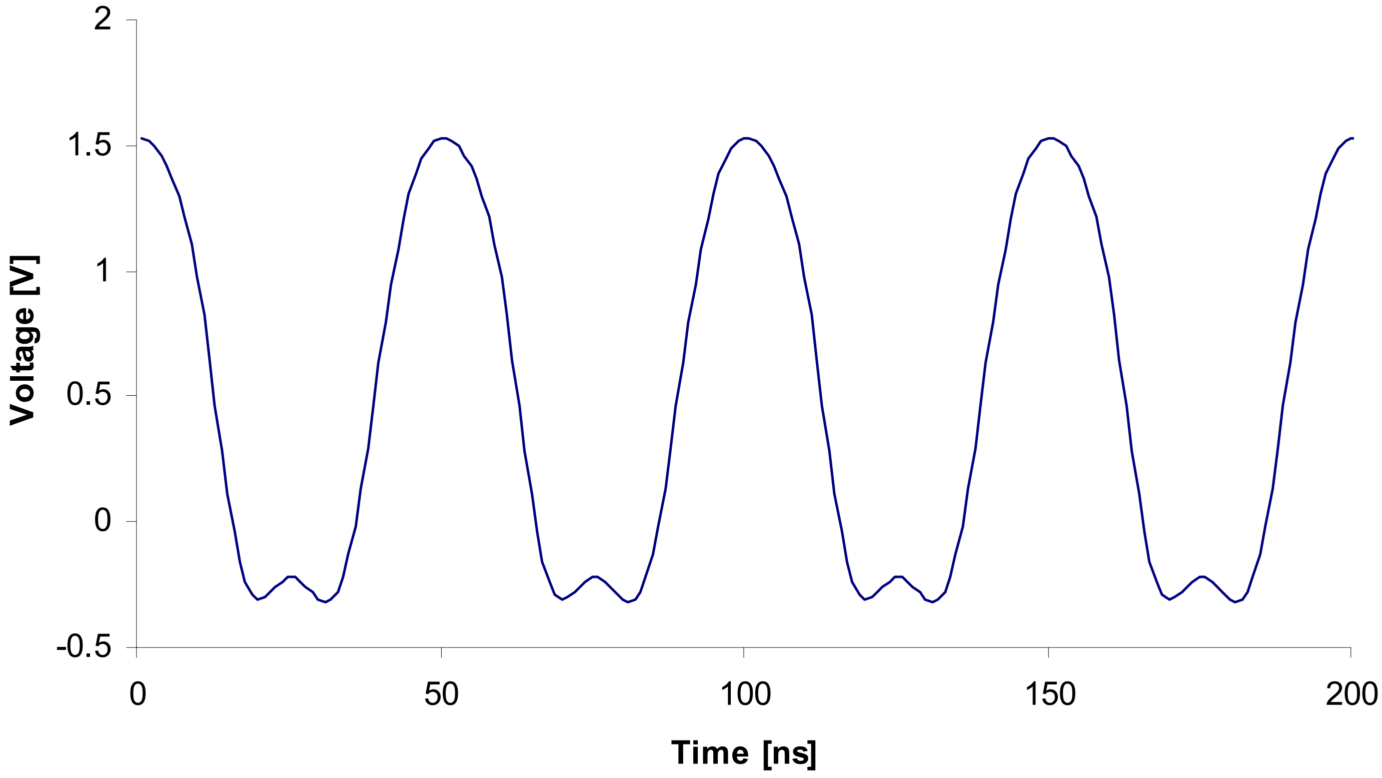
# Input Impedance at Microwave Frequencies: Dependence of Resonance on Input Bias



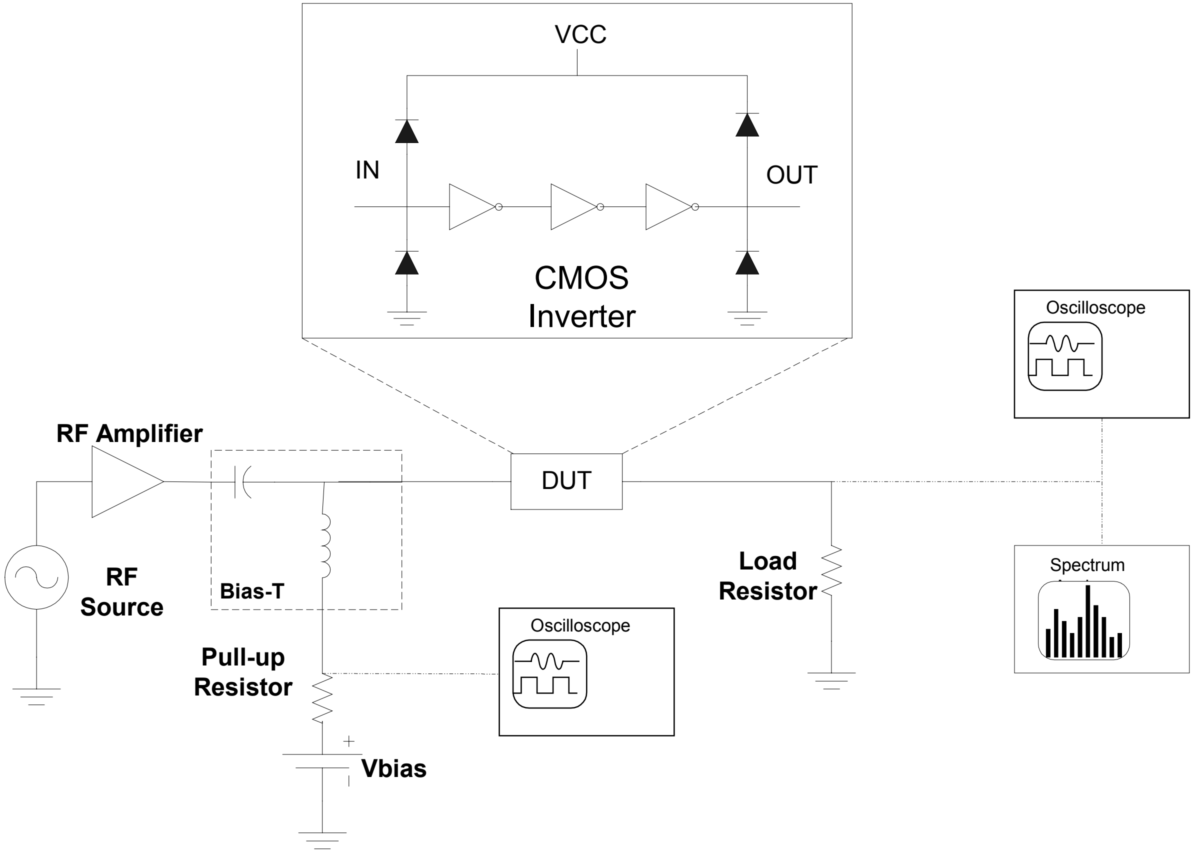
# LVX Family Input Impedance



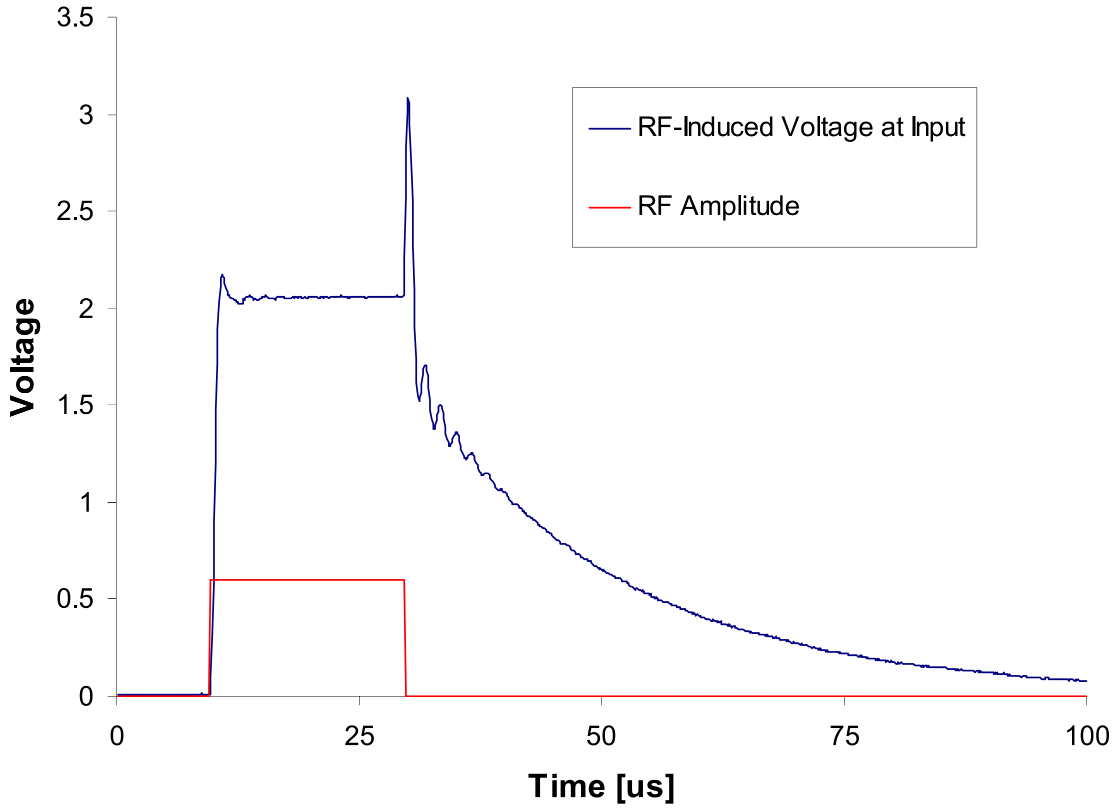
# Rectification of RF by Ground-Clamp ESD Diode



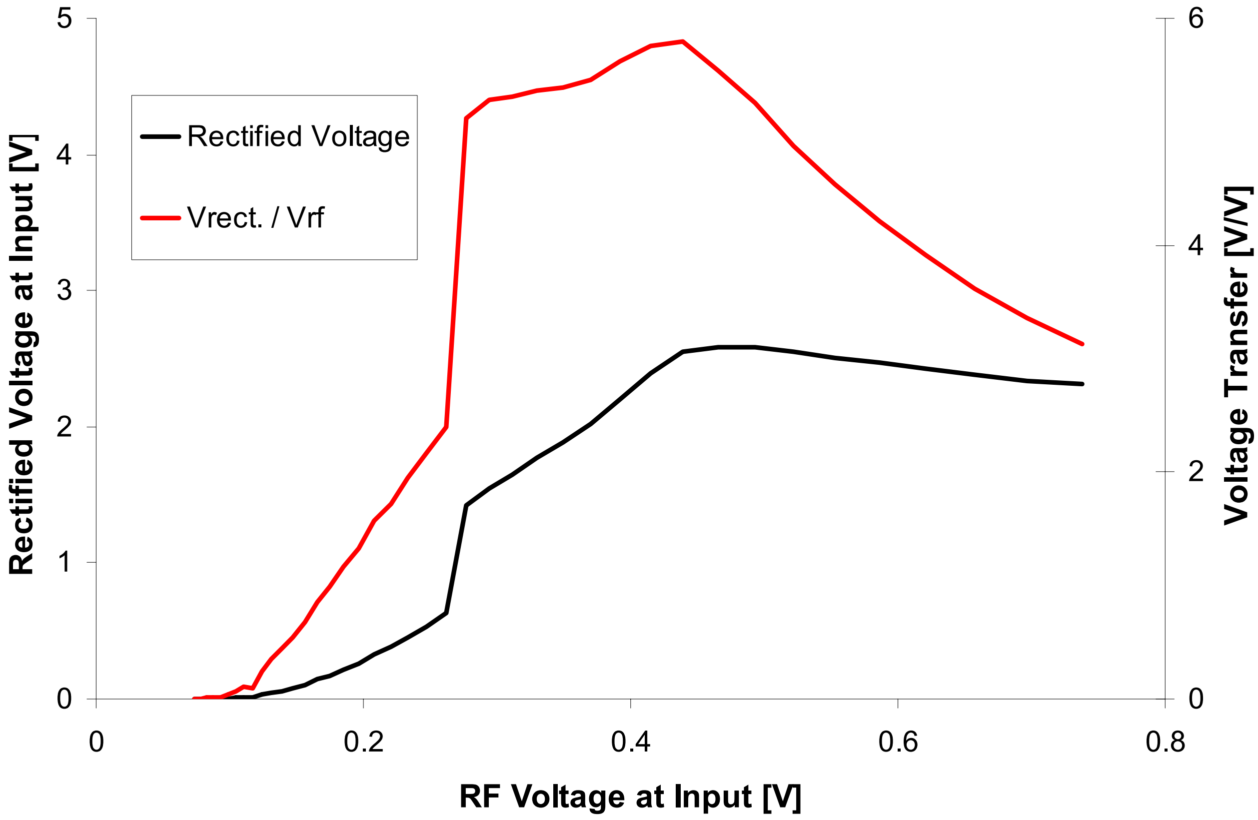
# Direct Injection RF Test System



# Voltage Induced at Input from Rectification of Microwave Pulse by ESD Diode (Frequency = 1.4 GHz, LVX Resonance)



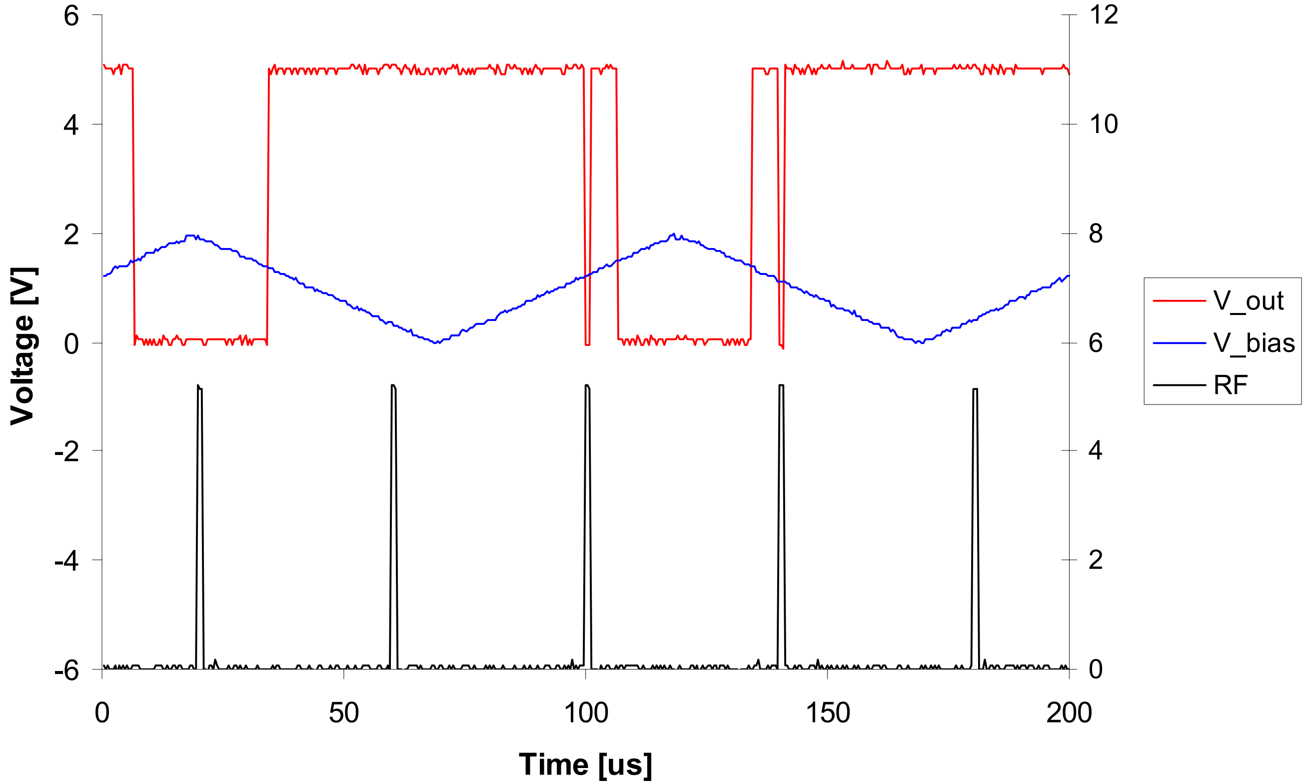
# Drive Characteristic of RF Rectification in ALVC
# (Frequency = 0.95 GHz, ALVC Resonance)



# ALVC Response as RF Amplitude Increases

09_rodgers_alvc.avi

# **Logic Rise Time Matters**: When Input Voltage is Near Switching Threshold, Device is Very Sensitive to RF



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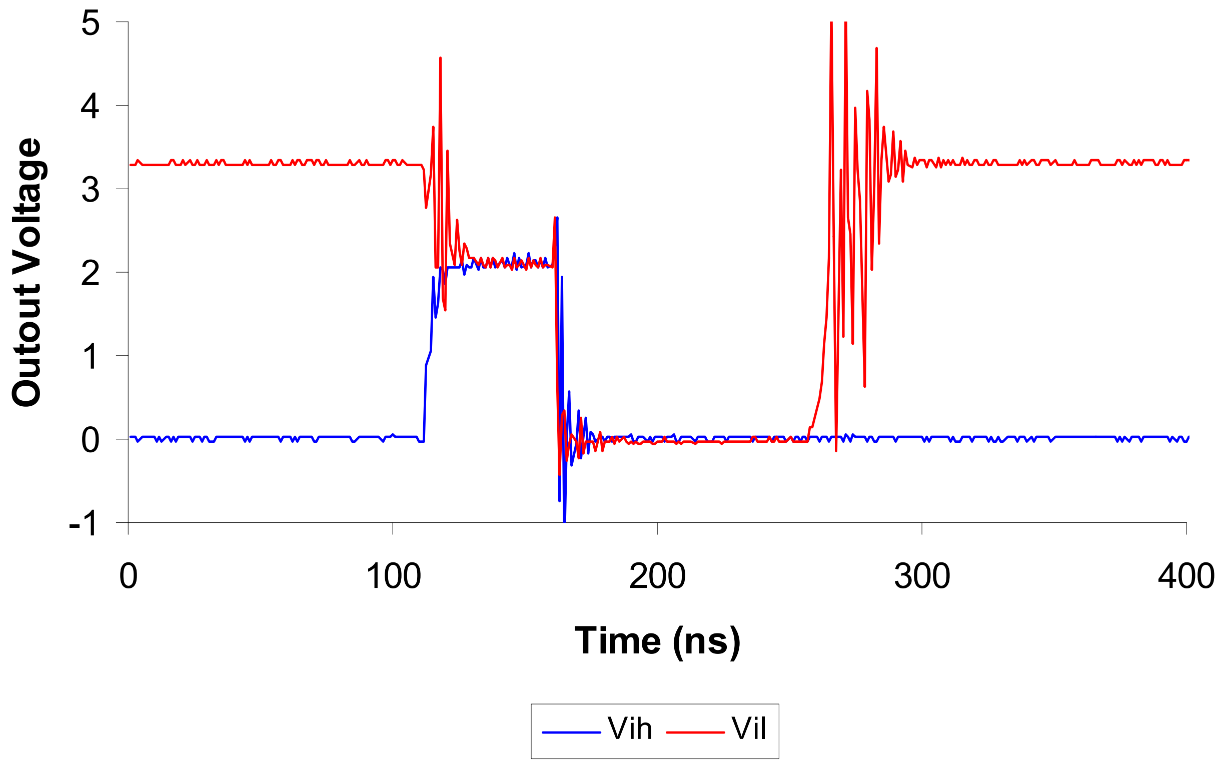
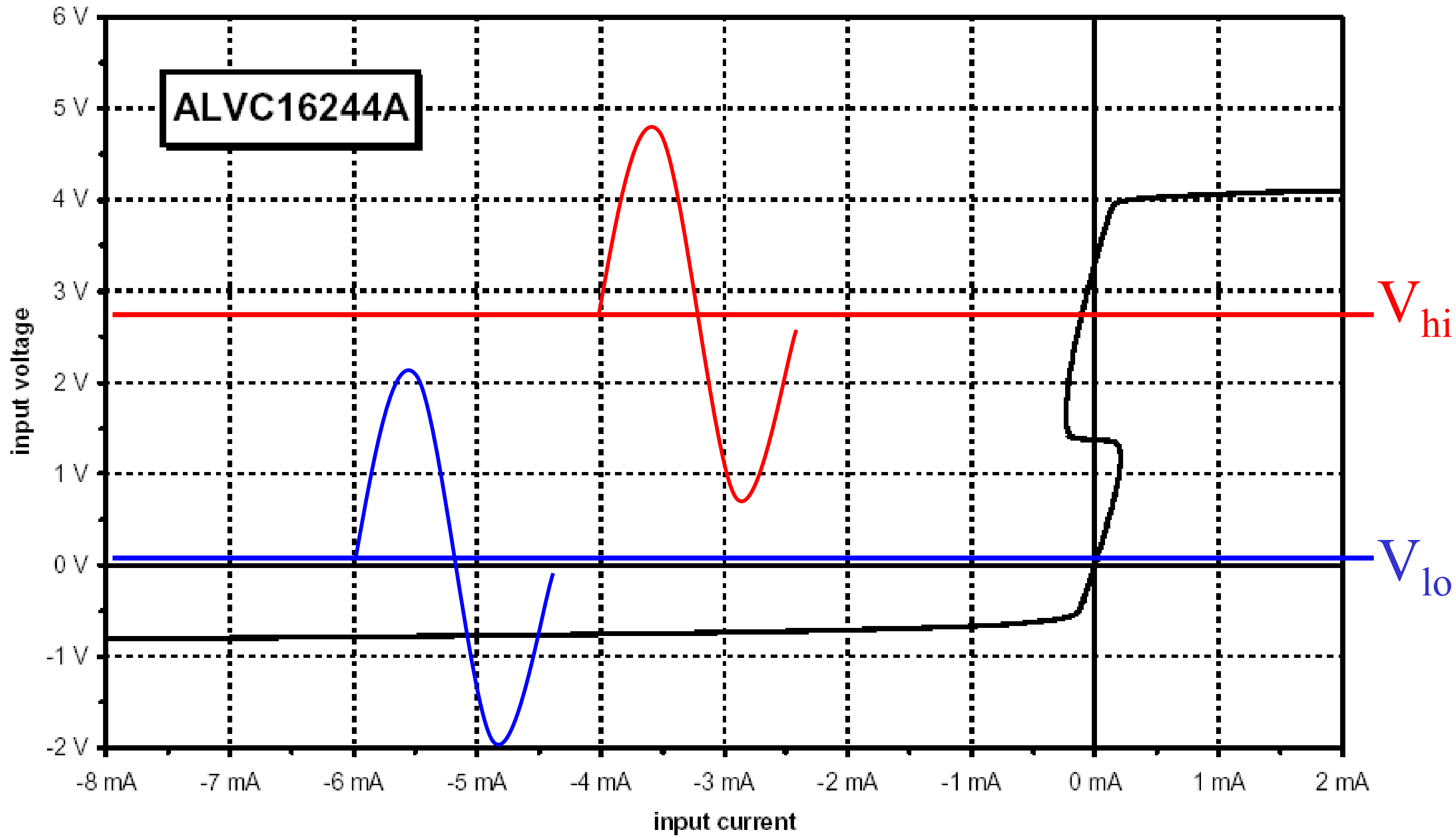
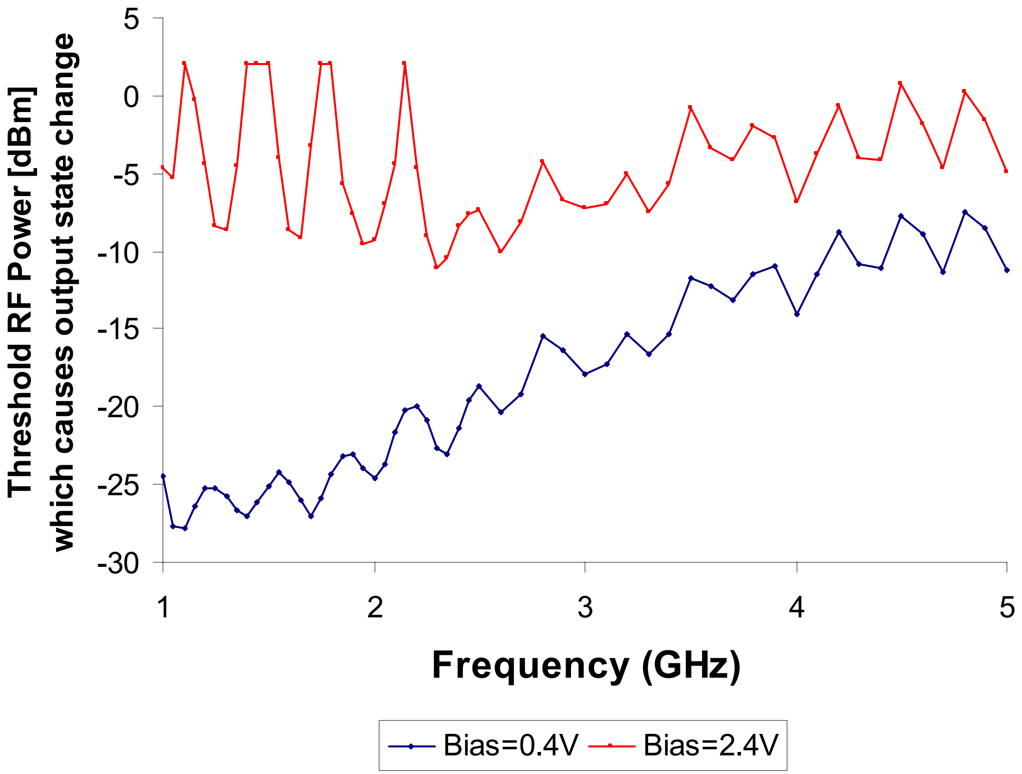
# **Input State Matters**: Comparison of ALVC Output Voltage with High and Low Input Levels and RF Excitation



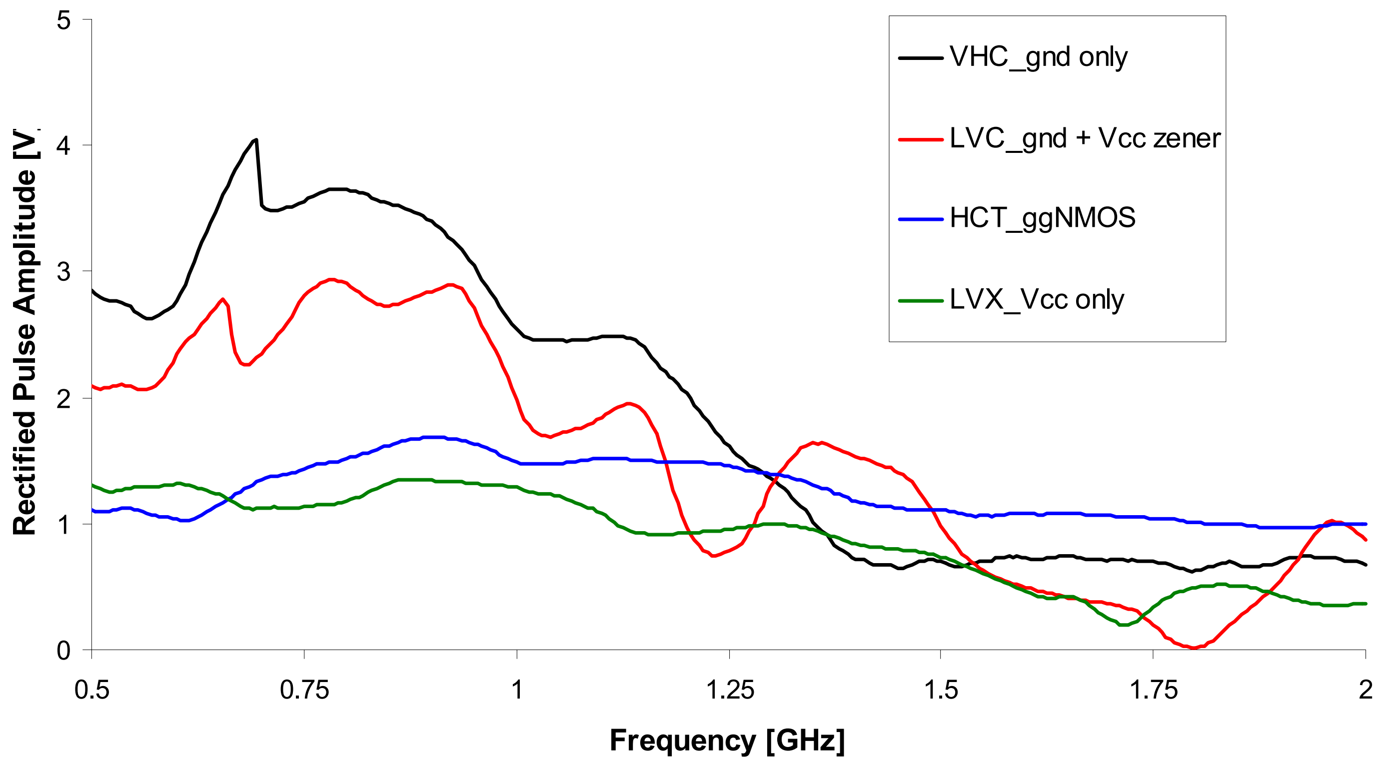
# Input IV Characteristics of ALVC (has both Vcc and ground clamp diodes)



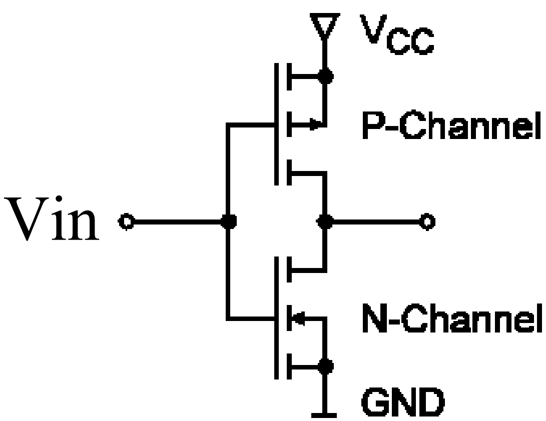
# **ESD Device-Type Matters**: Comparison of HCT Susceptibility with High and Low Input Levels (HCT grounded gate NMOS clamp)

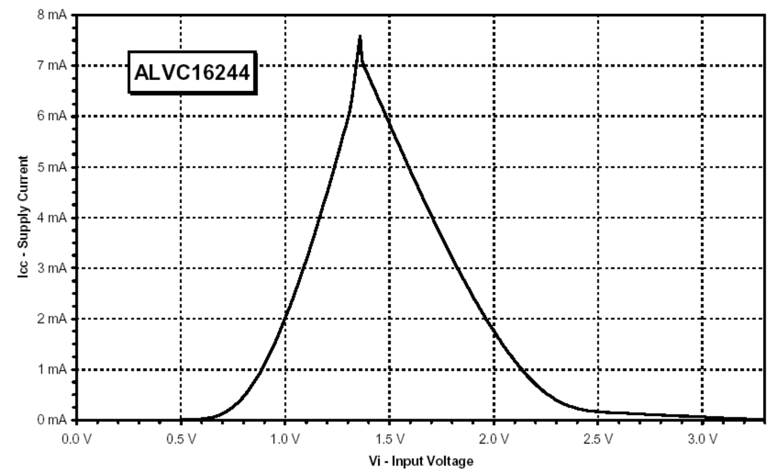


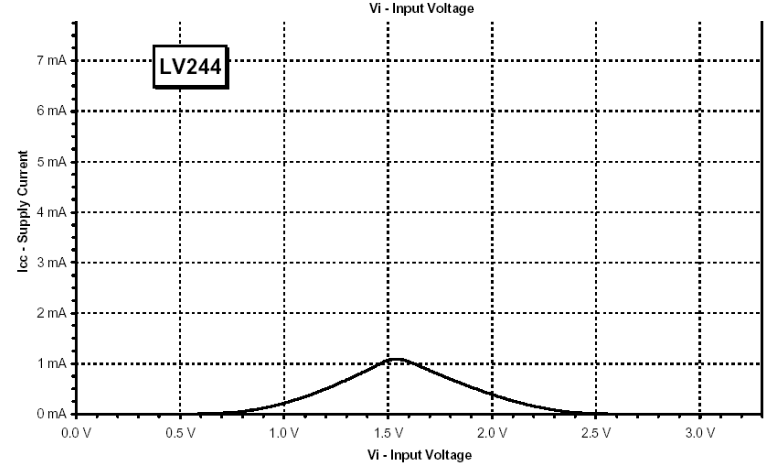
# **ESD Topology Matters**: Comparison of rectified pulse amplitudes in devices w/ ESD ground clamp, $V_{cc}$ clamp, and both (input biased low state)



# **CMOS Characteristics Matter**: Comparison of devices with wide and narrow input voltage bands where both MOS transistors are conducting

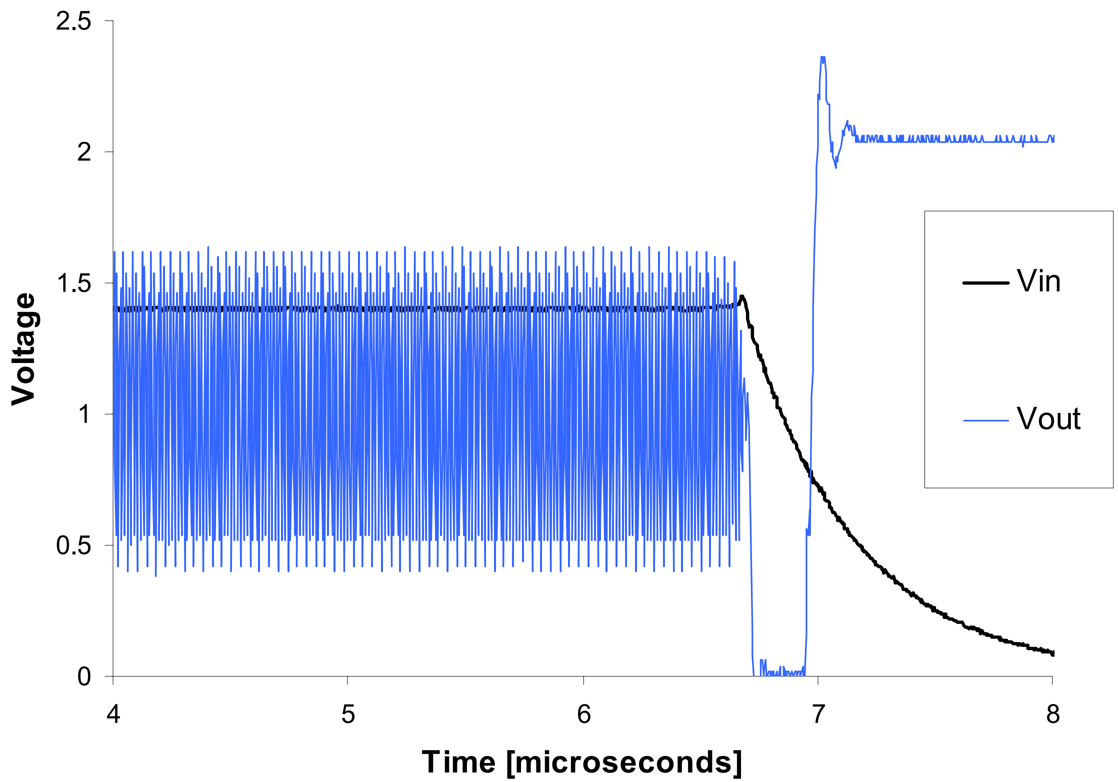


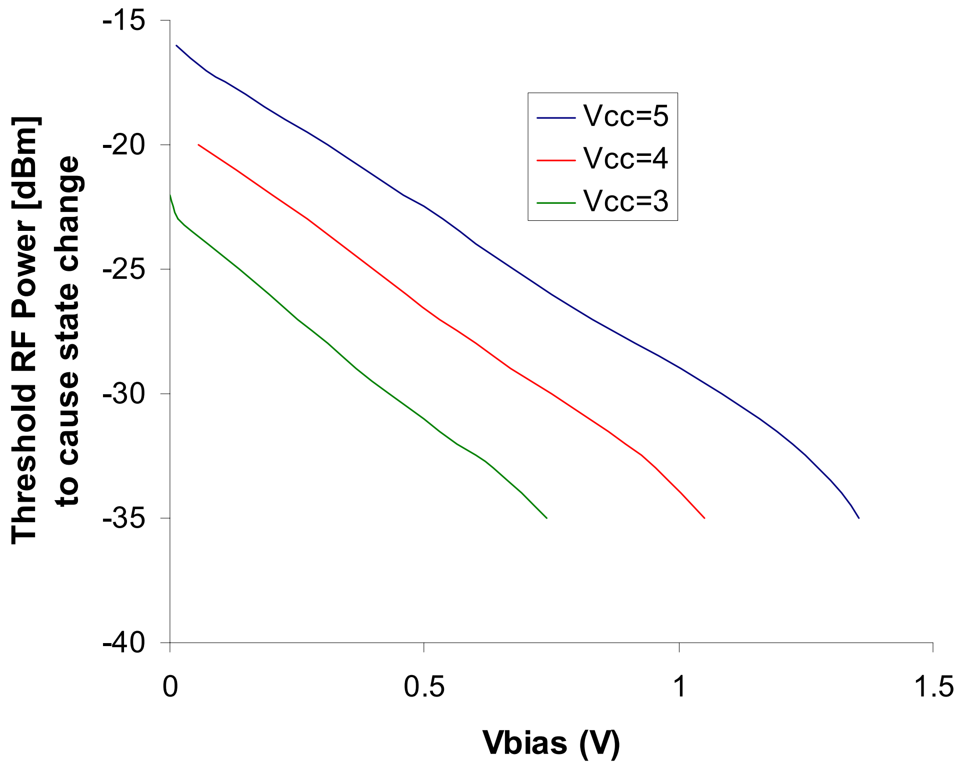



When RF biases both CMOS transistors into conduction, device becomes unstable and noisy. Other nonlinear effects have also been observed (possibly chaotic oscillations).

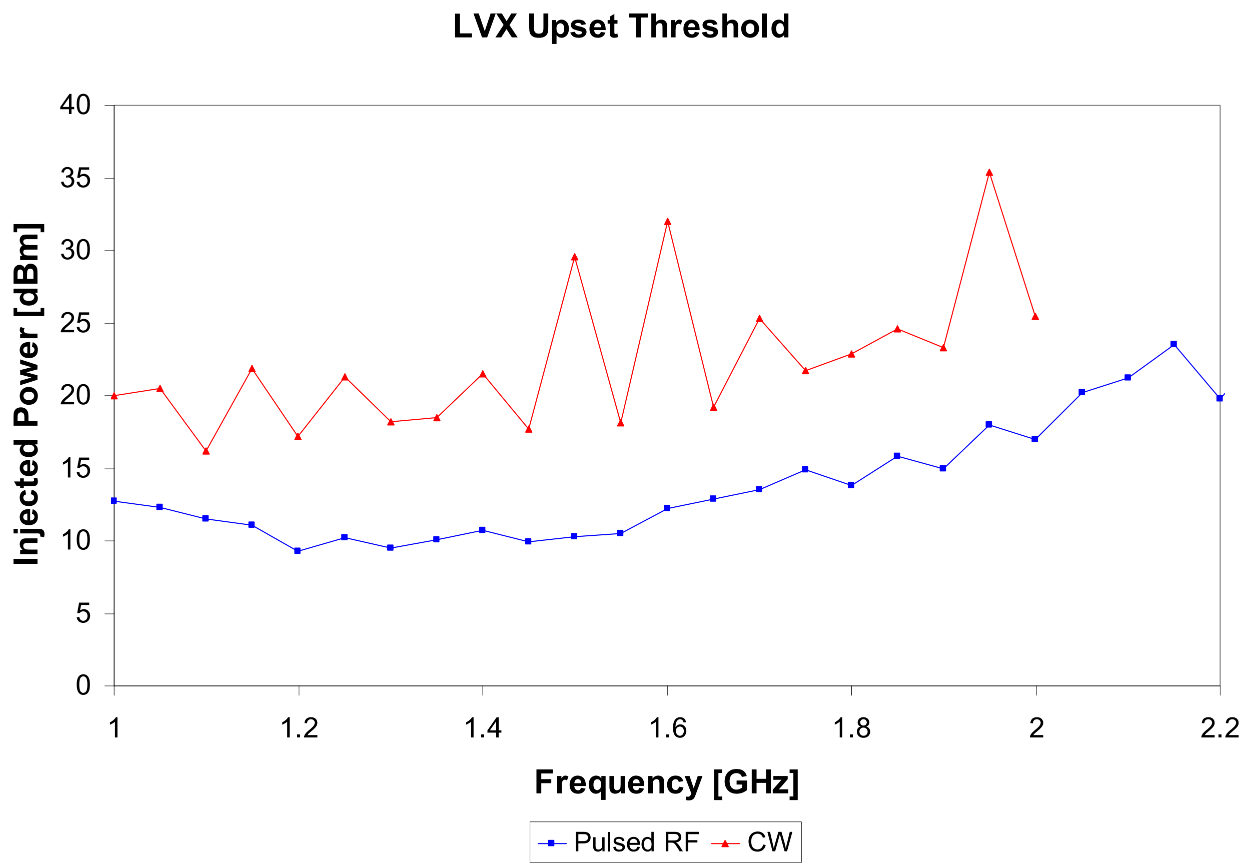
**Tail End of LVX Input and Output Voltages as RF Pulse Terminates**



**Operating Voltages Matter:** Typically, devices are more susceptible to RF as Vcc decreases and the switching (threshold) voltage band narrows.



# **Modulation Matters**: Comparison of CW and Pulsed Excitations at Same Power Level



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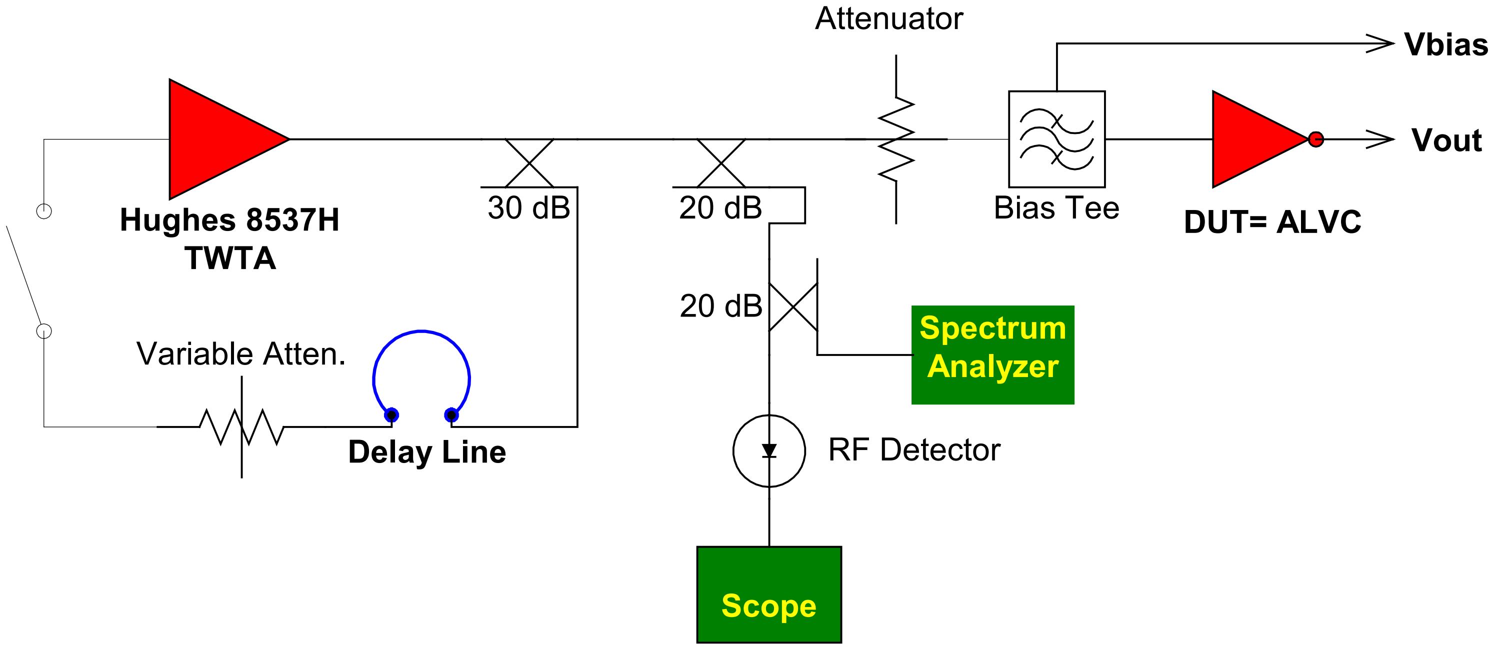
# Injection of RF Pulse with Chaotic Amplitude



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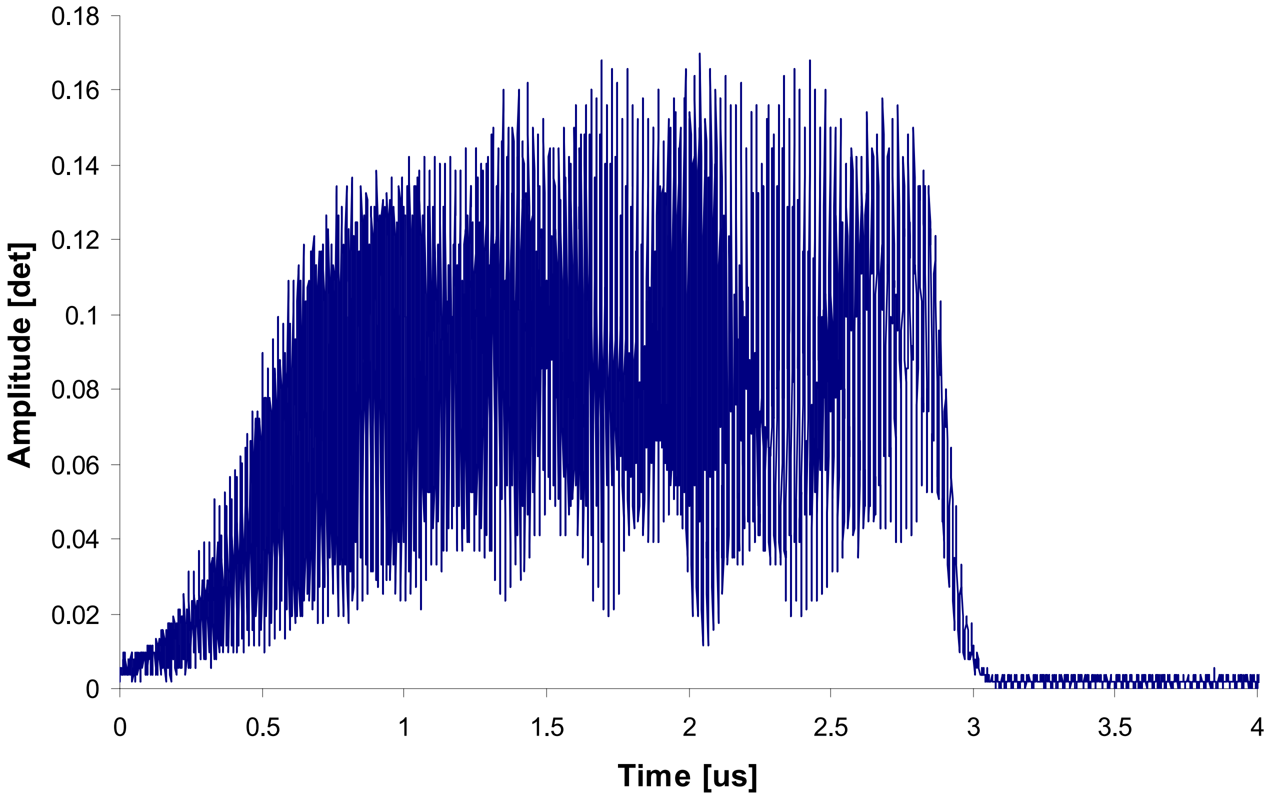
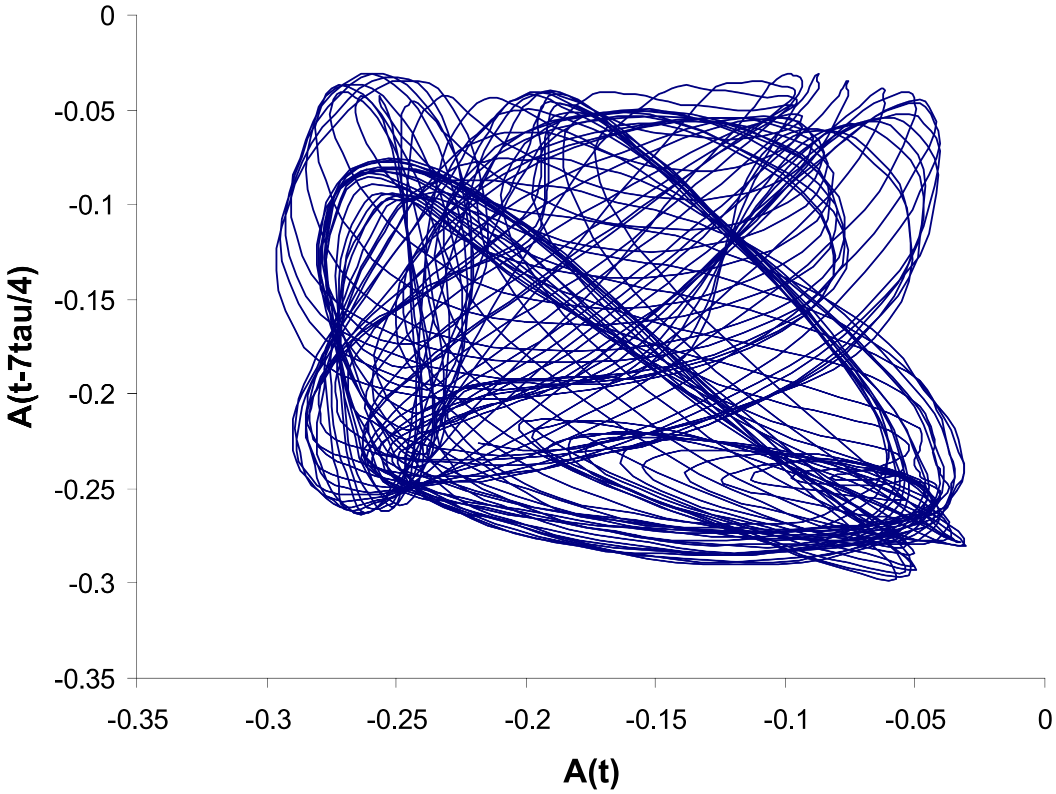
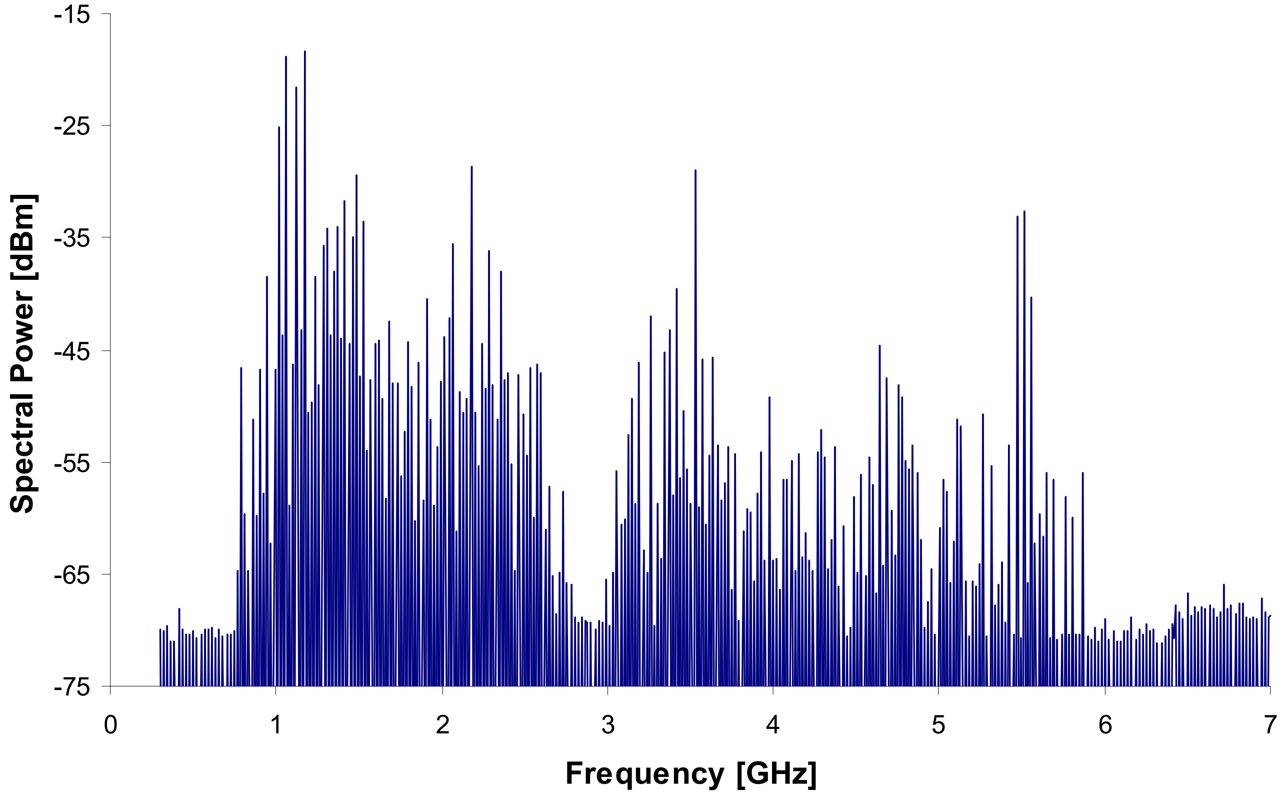
# Amplitude of TWT Output



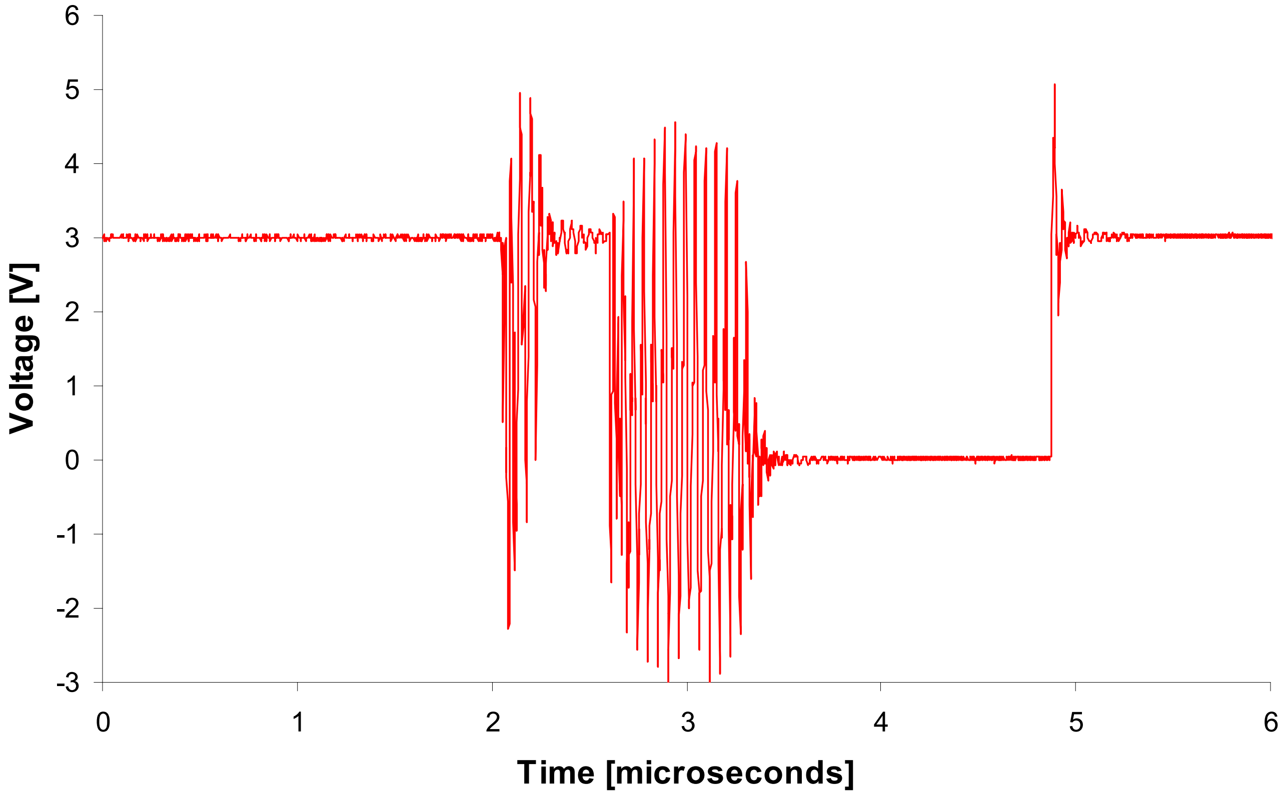
# Attractor Map of TWTA Amplitude



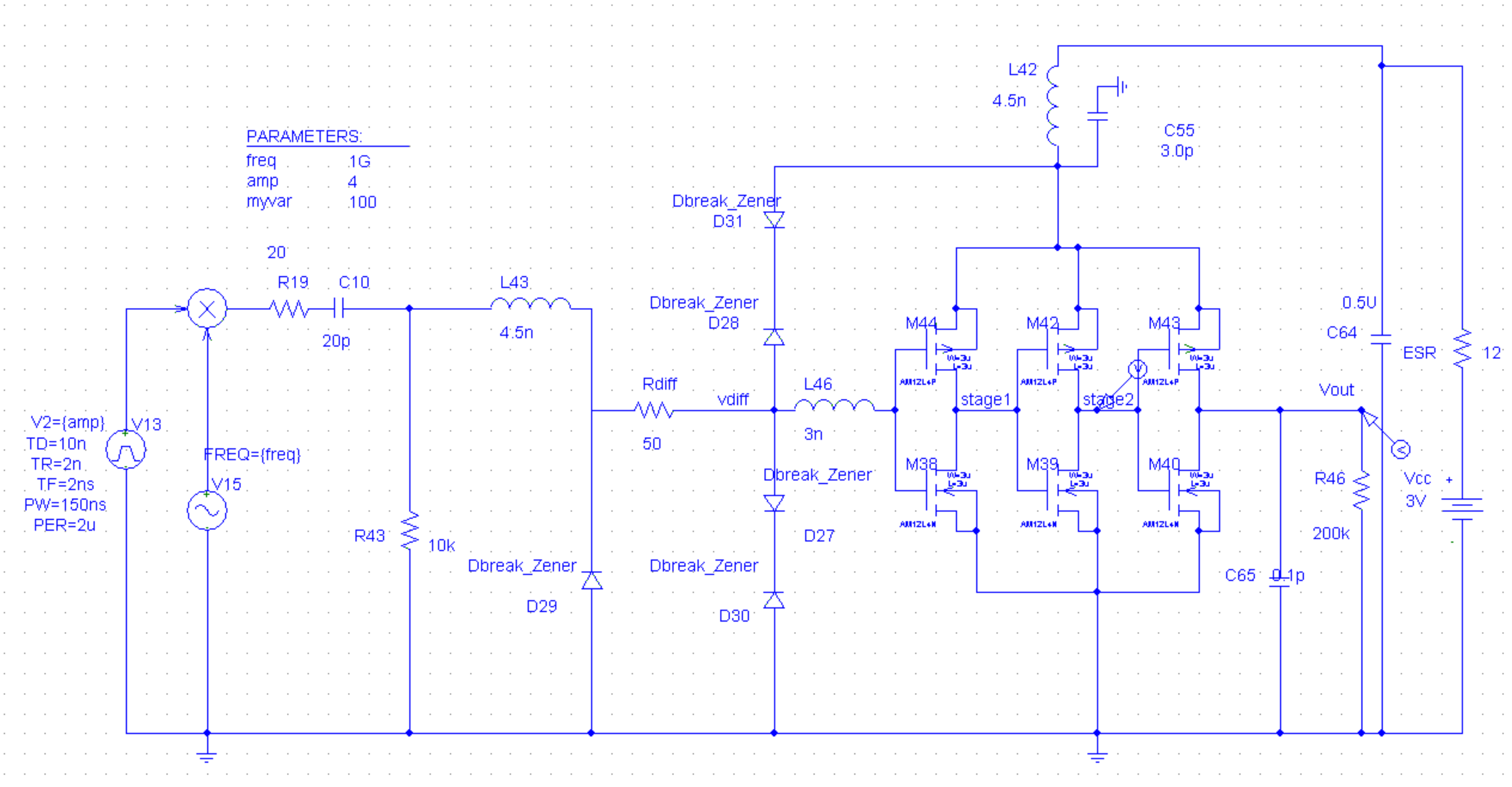
# Spectrum of RF Pulse from TWT



# Output of ALVC Device w/ “Chaotic” Input



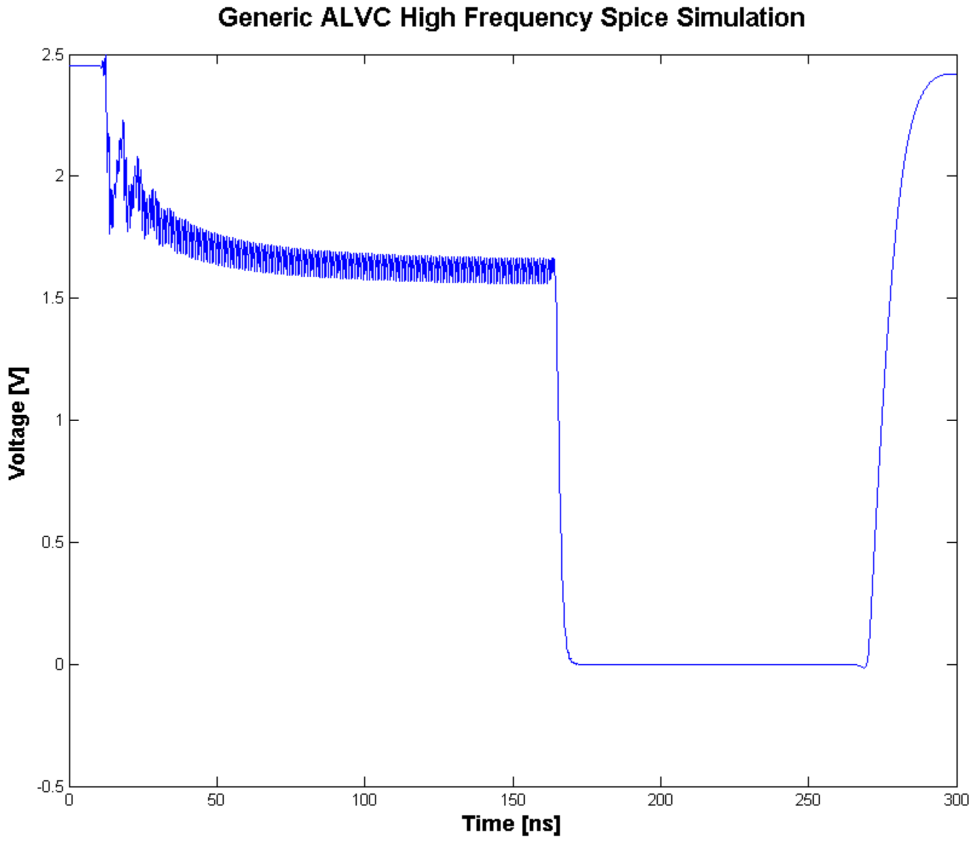
# High Frequency Spice Modeling



# Spice model includes:

- Package and bonding parasitics
- High frequency characteristics of Vcc bypass capacitor: inductance, ESR
- ESD diodes: reverse recovery, $C_j(V)$, $R_f$, etc.
- External parasitics on ground and Vcc buses.

# Spice simulation of ALVC output voltage with input excited by RF pulse



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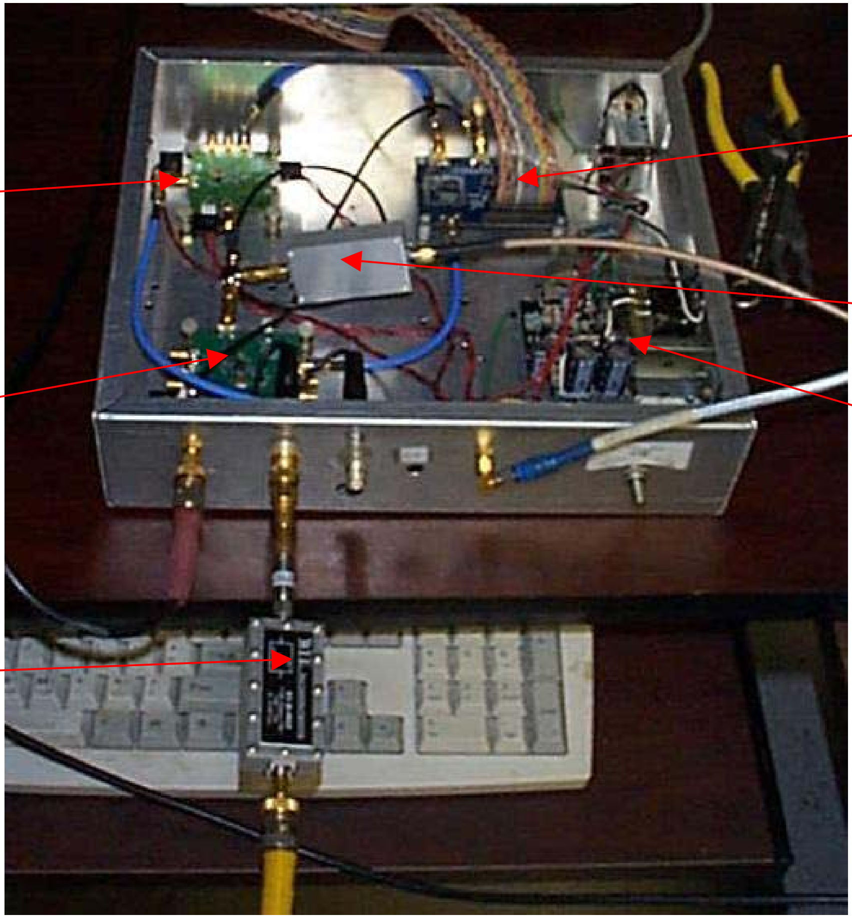
# Studies of RF Effects in Wireless Communications and Mixed Signal Systems (e.g. Bluetooth)



RF Amp/ Mixer

Demodulator

Baseband Output

Synthesized LO

RF Pulse Input

Power Supply

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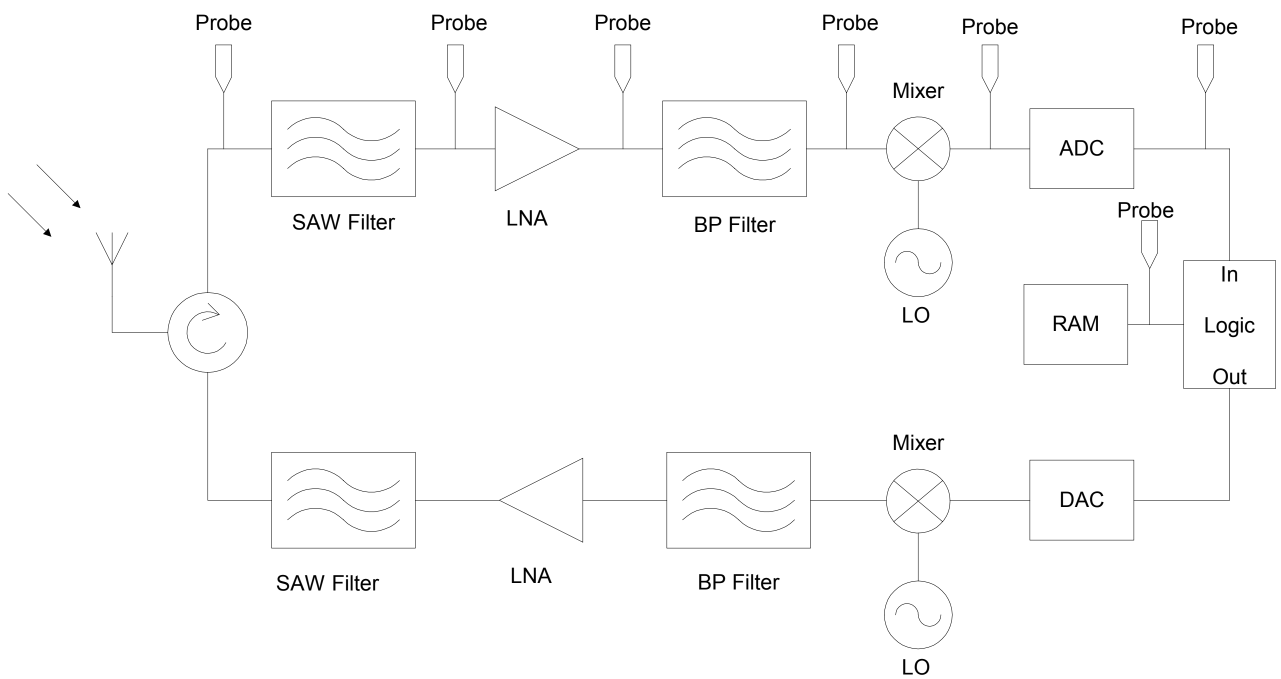
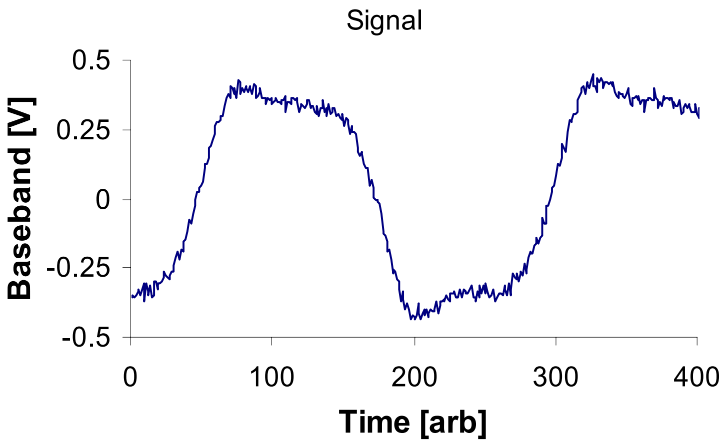
# Schematic of a “loop-back” test circuit for investigating RF effects in digital communications systems and components

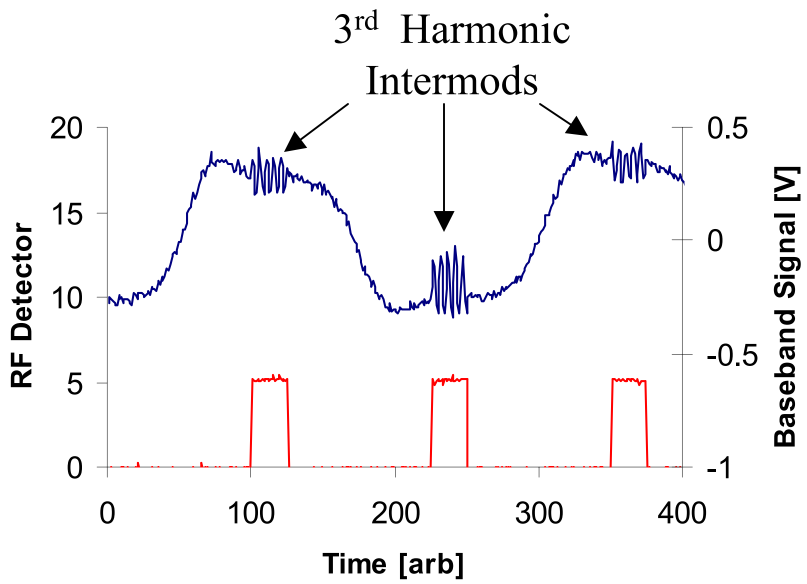



Find possible RF entry points, pathways and circuit effects that may upset the system or corrupt data.

# RF Effects on Baseband “Bluetooth” Signal




No RF Pulse

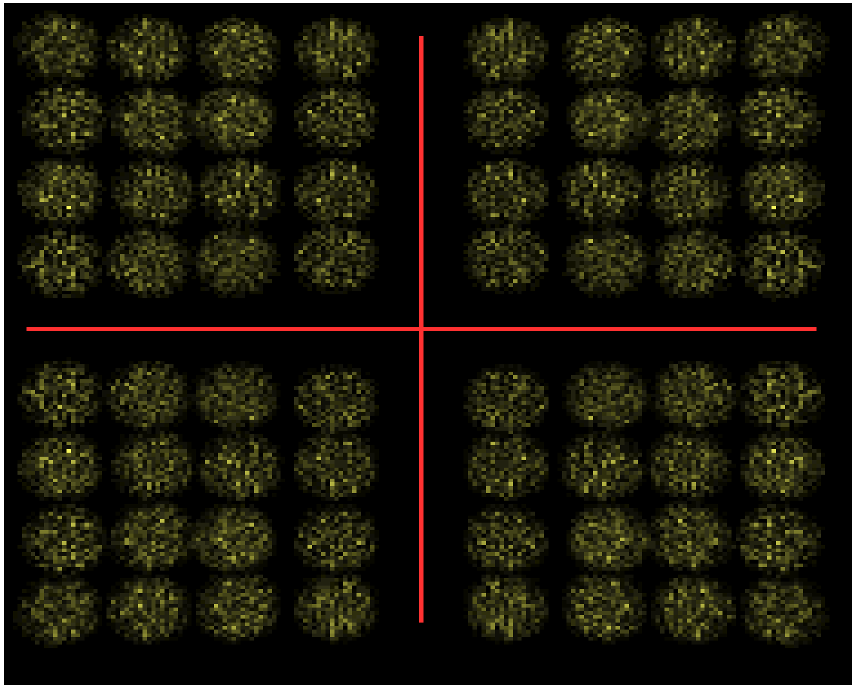



With RF Pulses

# The Effect of Noise on Digital RF Signals

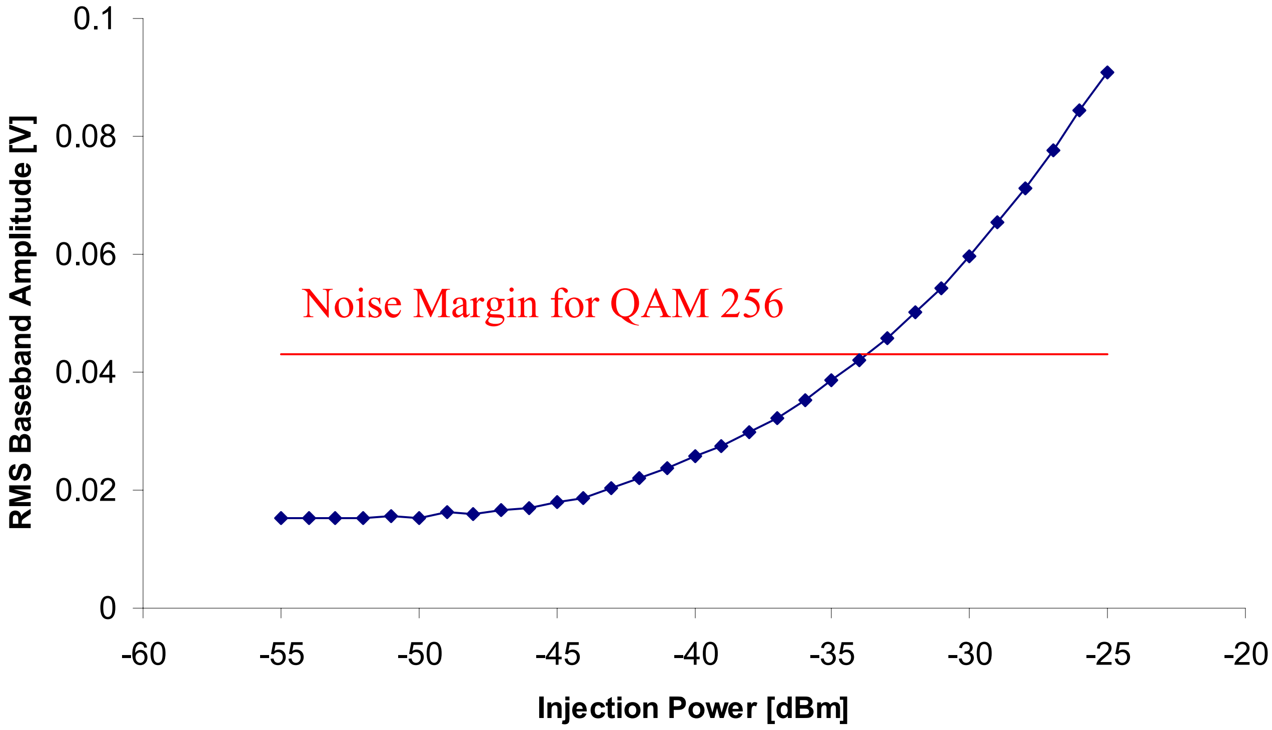
Digital communications signal plus noise or interference:

$$V(t) = (V_0 + V_M[t] + V_N(t))e^{-j(\omega t + \phi[t] + \Phi_N(t))}$$



Noisy QAM 64 Constellation

# Results of 3rd Harmonic Injection (1.129 GHz at IF Stage)




Plot of RMS amplitude of the baseband interference signal vs. RF pulse power.

# Summary of Results

- RF pulses are detected by nonlinear circuit elements.
- Susceptibility depends on ESD type and topology, parasitic resonances, bias and supply voltages.
- Demodulated RF pulses mimics valid logic states and cause state change.
- Faster, smaller, lower voltage devices are more susceptible at low power levels and higher frequencies.
- Susceptibility enhanced by parasitic resonant frequencies, which increase as operating speed increases.
- Other nonlinear effects (bias shift, oscillation, noise) disrupt data even if output state does not latch.

# Collaborations

- Jaycor/Titan interested in results for model development
  - Visit resulted in agreement to share experimental data.
  - First installment CD sent 10/03 containing test result for most advanced CMOS families.
  - Second installment will be sent by 12/03 containing general high frequency device characteristics.
- MRC has expressed interest in possible collaboration.
- Philips Semiconductor:
  - UMD requested information on Phillips ESD circuits.
  - The Phillips Engineering Applications chief contacted UMD to arrange a phone meeting to discuss possible collaboration. He expressed extreme interest in the project.
  - Phillips and UMD will be executing a nondisclosure agreement whereby they will share proprietary design data on ESD.
  - They recently sent us proprietary SPICE models and an internal handbook on modeling high frequency package parasitics.

# Future Work

- Continue expanding the experimental/empirical basis for modeling high frequency effects in devices (BiCMOS, LinBiCMOS).
- Develop generalized formalisms which account for parasitic reactance, diode response, high order nonlinearity (charge conservation models).
- Further investigate effects from complex (esp. chirp), chaotic and ultra-wideband modulation of RF pulses.
- Look at smaller, faster structures (CPU core, RDRAM, DDR, etc.) to verify scaling laws.
- Investigate RF effects in mixed signal systems (A/D, demodulators, etc.).